DØ Run 2B Silicon Detector Upgrade

Technical Design Report

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CHAPTER 1 - INTRODUCTION

The current DØ silicon tracker was built to withstand the 2 – 4 fb^{-1} of integrated luminosity originally projected for Run 2. Because of the tantalizing physics prospects a higher integrated luminosity brings, the laboratory supports extended running of the Tevatron collider, called Run 2B, which would deliver a total integrated luminosity of 15 fb^{-1} over the course of the full Run 2. However, the higher integrated luminosity now scheduled for Run 2B will render the inner layers of the present silicon tracker inoperable due to radiation damage. Of particular importance to being able to collect the data needed to exploit the physics potential of the Tevatron is the completion of a replacement of the silicon detector in approximately three years with minimal Tevatron down time. The DØ collaboration carefully studied two options for a Run 2B silicon tracker replacement: "partial replacement" and "full replacement." In the partial replacement option, the present tracker design is retained and the inner two silicon layers are replaced with new radiation tolerant detectors. In the full replacement option, the entire Run 2A silicon tracker is replaced with a new device. An internal review of these two options identified significant risks with the partial replacement option. These include the risk of damage to the components not being replaced, the long down-time required to retrofit the existing detector, an inadequate supply of the SVX2 readout chips, difficulties in adequately cooling the inner layers, and marginal radiation hardness for the extended operation of Run 2B in the layers not being replaced. Furthermore, it is nearly impossible to re-optimize the detector for the Run 2B physics program with the partial replacement option. For these reasons, DØ decided to proceed with the full replacement option for Run 2B and build a new silicon tracker that is optimized for the Higgs search and other high-p_T physics processes.

The design studies for the new silicon detector were carried out within a set of boundary conditions set by the Laboratory and derived from the physics goals for Run 2B. The first requirement imposed is that the detector be able to withstand an integrated luminosity of 15 fb^{-1}. For 15 fb^{-1}, combining the data of both the CDF and DØ detectors, a 5σ discovery of the Standard Model Higgs can be made for a Higgs mass of 115 GeV, a $>3\sigma$ signal is expected for most of the mass range up to 175 GeV, and Higgs masses up to 180 GeV can be excluded if there is no sign of the Higgs. This result depends crucially on the ability to efficiently tag b-jets, which drives the detector design towards placing the silicon detectors at relatively small distances from the beam. Being able to collect this high an integrated luminosity with the tracking device so close to the interaction point puts stringent requirements on the cooling for the inner layers and has led to a natural division of the detector into two radial groups, an inner and outer group. The laboratory has required that the shutdown for replacement of the current silicon detectors should occur in the year 2004 and should not exceed six months in duration. This timeframe is set by the startup of the LHC collider at CERN. This stringent timetable forces the detector to be replaced in the DØ collision hall. A rollout of the detector, out of the collision hall into the assembly hall, replacing the silicon detector, and rolling it back in is an operation estimated to take at least nine months and would inevitable engender a larger effort. Installation of the new silicon detector in the collision hall constrains the installable package length to 52", determined by the space available between the central and end calorimeters in the collision hall which is only 39". The last requirement imposed by the Laboratory is that the project should be completed within a tight budget. To reduce the cost and to keep to the schedule as much of the present data acquisition system as possible will be retained. Even though there are significant

boundary conditions, the new detector presented in this document is designed to have better performance than the Run 2A detector and is expected to be completed within the allocated time, calling for an installation in the summer of 2004.

This report describes the current conceptual design of the new silicon detector for the DØ experiment for Run 2B. Chapter 2 briefly summarizes the physics motivation for an extended run of the Tevatron. Chapter 3 gives an overview of the proposed DØ silicon detector design and serves as an introduction to the next chapters. Chapter 4 discusses the silicon sensors, chapter 5 the mechanical aspects of the design, chapter 6 the readout electronics. Chapter 7 describes the production and testing, followed by chapter 8 which will describe the software needed for the quality assurance and testing of the devices. In chapter 9 an overview of the expected performance based on simulations is presented and chapter 10 presents the cost estimate. A summary is given in chapter 11. The document includes an appendix that describes the overall management structure of the Run 2B Upgrade Project. At the time of writing this report, full closure has not been reached on all aspects of the design. As such, particular features will necessarily change if deemed to improve on the current design. Nevertheless we are confident that this design forms a solid basis for proceeding to construction of a detector capable of meeting the Run 2B physics goals.

CHAPTER 2 - PHYSICS GOALS

Proton-antiproton collisions at $\sqrt{s} = 2$ TeV have proved to be a very fruitful tool for deepening our understanding of the standard model and for searching for physics beyond this framework. DØ has published more than a hundred papers from Run 1, including the discovery and precision measurements of the top quark, precise tests of electroweak predictions, QCD tests with jets and photons, and searches for supersymmetry and other postulated new particles. With the addition of a magnetic field, silicon and fiber trackers, and substantial upgrades to other parts of the detector, DØ has started Run 2 with the goal of building on this broad program, taking advantage of significantly higher luminosities, and adding new measurements in b-physics. The strengths of the DØ detector are its liquid argon calorimetry, which provides outstanding measurements of electrons, photons, jets and missing E_T; its large solid angle, multi-layer muon system and robust muon triggers; and its state of the art tracking system using a silicon detector surrounded by a fiber tracker providing track triggers.

A series of physics workshops organized by Fermilab's Theory group together with the CDF and DØ collaborations has mapped out the physics terrain of the Tevatron in some detail. It is clear from the very large amount of work carried out in these meetings and described in the reports[1] that integrated luminosities much higher than the $2fb^{-1}$, which was the original goal of Run 2 add significantly to the program. While all areas of physics benefit from increased statistics, it is the very real possibility of discovering the standard model Higgs boson (or its supersymmetric versions) and/or supersymmetric particles or other physics beyond the standard model, that forms the core motivation for the Laboratory's luminosity goal of 15 fb^{-1} per detector. We have therefore used the most promising Higgs discovery channels as benchmark processes for the silicon detector upgrade, which is described in this Design Report, and have optimized the detector configuration for them. All other high p_T physics programs benefit from this detector optimization, (though for the QCD and b-physics programs the benefits will be balanced by decreased trigger efficiencies and geometric acceptance). In the following, we discuss physics requirements on the tracking system imposed by Higgs searches and their implications for other high p_T physics programs.

2.1 Standard Model Higgs Boson Searches

The dominant Higgs production channel at the Tevatron is the gluon fusion reaction $gg \rightarrow H$. Unfortunately, for Higgs masses below about 135 GeV, its dominant decay mode is to bb and is swamped by QCD production of b-jets. The most promising Higgs search strategy in this mass range is to focus on associated production of a Higgs with a W or Z boson, $\bar{p}p \rightarrow WH$ and $\bar{p}p \rightarrow ZH$. The leptonic decays of the W and Z enable a much better signal to background to be achieved, but one must pay the cost of a production cross section about one fifth that of inclusive production together with the leptonic branching ratios of the vector bosons. This relatively low signal cross section times branching ratio motivates the need for high integrated luminosity. In turn, the need for high integrated luminosity forces the accelerator to operate in a mode where each high p_T event is likely to be accompanied by a significant number (<n>=6) of low p_T "minimum bias" events occurring in the same $p\bar{p}$ bunch crossing. This high occupancy environment is one of the main challenges in tracker design for Run 2B.

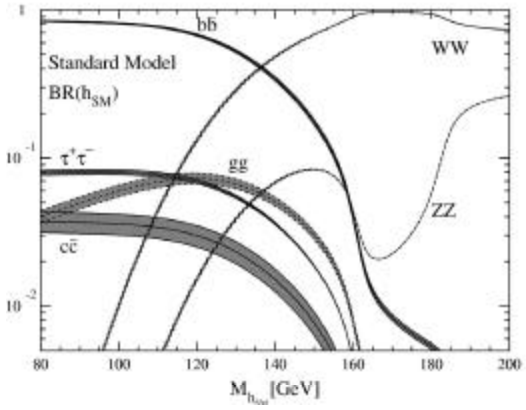

Figure 1 - Standard Model Higgs decay branching ratios as a function of Higgs mass.

Figure 1 shows the decay modes of the Standard Model Higgs in the mass range relevant to DØ. For Higgs masses below roughly 135 GeV, the Higgs decays dominantly to b-quark pairs, and for masses above this (but less than the $t\bar{t}$ threshold) the decay is dominantly to W and Z boson pairs. Thus, searches for Higgs boson in the low mass region $M_H < 135$ GeV must assume $H \rightarrow b\bar{b}$ decays. Searches for the lightest Higgs in supersymmetric models must also assume decay to b-quark pairs.

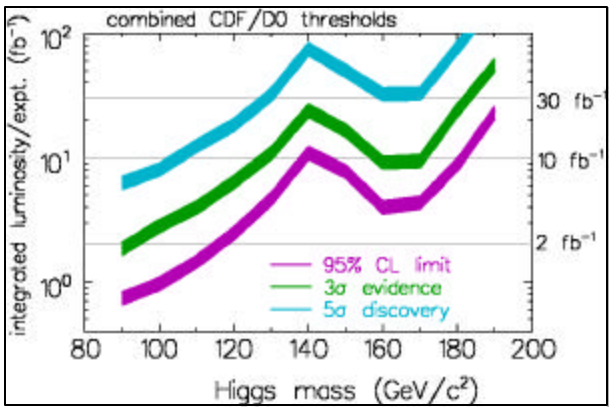

Figure 2 - Required luminosity as a function of Higgs mass for 95% C.L. exclusion, 3 s evidence, and 5 s discovery.

Figure 2 shows the luminosity required to exclude or discover a Standard Model Higgs at the Tevatron. This result assumes the expected Run 2A performance of both the CDF and DØ detectors. For 15 fb^{-1}, a 5σ discovery can be made for a Higgs mass of 115 GeV, a $>3\sigma$ signal is expected for most of the mass range up to 175 GeV, and Higgs masses up to 180 GeV can be excluded if there is no sign of the Higgs.

As stated above, for Higgs bosons in the low mass range, the associated-production modes will be used for searches. The final states of interest are those where the W(Z) boson decays to charged leptons or neutrinos, and at least two b-flavored hadronic jets from the Higgs decay are selected. The dominant background arises from W(Z) bosons produced in association with jets from initial state radiation of gluons. Even in the associated production channels, the intrinsic

signal to background for vector boson plus two jets is prohibitively small. However, the majority of the W(Z)+jets background contains light quark or gluon jets, while the Higgs signal is almost exclusively bb. The ability to identify the b-jets from Higgs decay is the crucial first step in reducing the boson+jets background to a manageable level. The combination of b-jet identification, reconstructed dijet mass, and additional kinematic variables is used to improve the signal to noise to achieve the sensitivity shown in Figure 2. This result depends on the ability to identify b-jets with at least 50% efficiency and background contamination from light quark jets at the 1% level. Effective tagging of b-jets is one the most important physics objectives for the tracker system. It is likely that two tagged jets will be required to reduce the background to acceptable levels, so maximzing the tagging efficiency is most important.

The identification of b-jets can be done by exploiting either the relatively long lifetime of the b-flavored particles or by detecting leptons from semi-leptonic decay of b-quarks (or both). The first technique allows all decays to be considered, whereas the second method suffers reduced statistical precision because of the ~30-40% decay branching ratio of b-quarks to final states including leptons. The long lifetime of the b-quarks is reflected in a B-meson decay that occurs some distance from the primary beam interaction point. For b-flavored particles with energies expected from Higgs decay, the mean decay length is 2 mm, and the mean impact parameter is roughly 250 μm. Thus, efficiently and cleanly identifying these decays requires a detector with the ability to reconstruct tracks with an impact parameter resolution in the tens of microns. The most feasible technology for this is silicon microstrip detectors.

One of the low-mass Higgs signatures is particularly noteworthy: Higgs production in association with a Z boson, which decays into a neutrino-antineutrino pair, resulting in missing energy and two b-jets in the final state. One of the main strengths of the DØ detector is its good missing energy identification; yet to keep trigger rates under control the present threshold on the missing E_T trigger is about 35 GeV. A search for the Higgs boson in the ZH channel can certainly benefit from a lower trigger threshold. This can be achieved if information about displaced tracks is used at the trigger level. DØ plans to implement a Silicon Track Trigger ? STT ? in Run 2A. The Run 2B silicon detector will be compatible with the logic of this trigger.

Searches for the Higgs boson in the higher mass region $135<M_H<200$ GeV/c^2 assume directly-produced Higgs decaying to WW* and ZZ*, where at least one of the vector bosons decays to leptons. Effective lepton identification, essential for vector boson detection, is important for Higgs searches in both low and intermediate mass regions. The tracking system plays a crucial role in electron, muon and, arguably, tau lepton identification. Leptons from W and Z decays are fairly energetic, with $p_T>20$ GeV/c. Thus, the effective reconstruction of high p_T tracks is another important requirement to the tracking system.

Higgs production in association with $t\bar{t}$ has received a lot of attention recently[2]. Though low in cross section, this channel provides a very rich signature with leptons, missing energy, and 4 b-jets in the final state. B-jets produced in this process have higher energy than those in processes such as WH production. Tracks in such jets tend to be more collimated, emphasizing the need for robust pattern recognition in the high occupancy environment. Another challenge for this channel is ambiguity in b-jet assignment, which can be reduced if the charge of the b-quark can be tagged. Several methods for b-charge tagging have been developed so far, e.g. same side tagging, jet charge tagging. Having information about charge of tracks in the secondary and

tertiary b-decay vertices could be invaluable to improve purity of these tagging methods. This puts additional emphasis on precise impact parameter reconstruction.

It is important to note that Higgs searches at the Tevatron and at the LHC are complimentary to each other. While LHC experiments[3] emphasize the $gg \to H \to gg$ channel, where Higgs is produced and decays via loop diagrams, the Tevatron's emphasis is on tree-level production and tree-level decay. For a Standard Model Higgs the branching ratio to gg is very low, making it impossible to observe this channel at the Tevatron. However, some models predict a "bosophilic" Higgs, for which this decay mode is enhanced. Thus, high-energy photon identification is important for Higgs search beyond the Standard Model. Photon/electron separation is essential for high-purity photon identification. For this purpose the tracking system must ensure low fake track rate and a good momentum resolution.

2.2 Searches For Physics Beyond The Standard Model

Searches for SUSY and strong dynamics will benefit from the requirements imposed on the tracking system by the Standard Model Higgs searches. SUSY extensions of the Standard Model predict two Higgs doublets with five physical Higgs bosons – two neutral scalars, one neutral pseudoscalar and two charged bosons. The neutral bosons behave similarly to the Standard Model Higgs, but some cross sections might be enhanced, e.g. $b\bar{b}A, A \to b\bar{b}$ in a high $\tan b$ scenario. Efficient b-jet tagging and b-charge identification is essential for Higgs discovery in these channels, which contain four b-jets. The charged Higgs boson decays to $b\bar{c}$ or $t^{-}n$, depending on $\tan b$. Again, good heavy flavor tagging and tracking (for tau-lepton identification) are important. Studies have shown that the Tevatron can exclude almost the whole plane of SUSY Higgs parameters (m_A, $\tan\beta$) at the 95% level, if no signal is seen in 5 fb^{-1}, and can discover at least one SUSY Higgs at the 5 standard deviation level with 15-20 fb^{-1} per experiment.

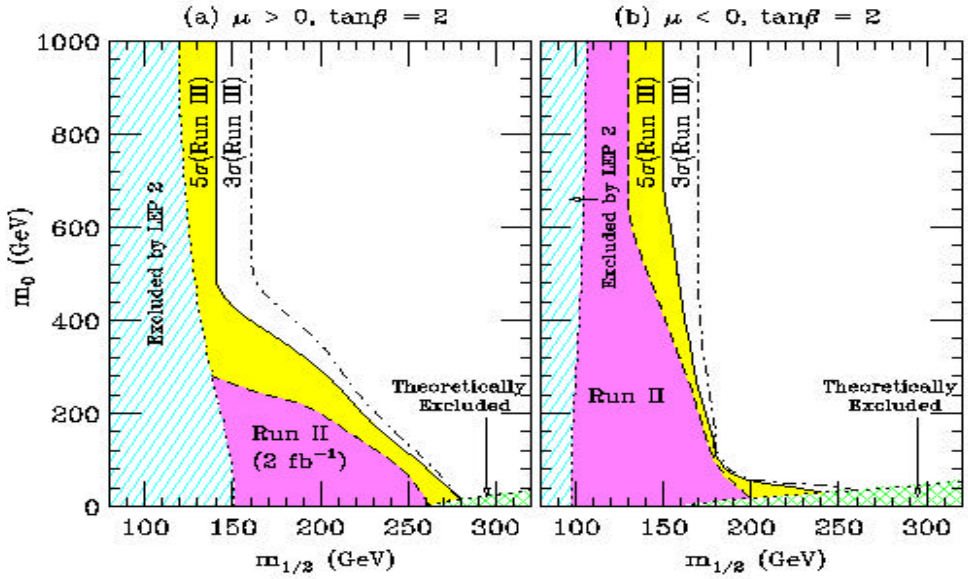

Figure 3 - Contours of 90% C.L. observation at Run 2A, 5σ discovery, and 3 s observation at Run 2B for $p\bar{p} \rightarrow \text{SUSY particles} \rightarrow 3l + X$ *in the* $(m_{1/2}, m_0)$ *plane for tanβ=2, (a)* $\mu>0$ *and (b)* $\mu<0$.

Direct searches for squark and gluino production, with jets and missing E_T signatures, have been carried out at the Tevatron since its inception. These still have an important role to play, but once a few inverse femtobarns have been collected, the limits will have reached 400-500 GeV on squark and gluino masses and further improvements will be limited because of the production kinematics. The greatest gains in going from 2 fb^{-1} to 15 fb^{-1} will likely come in searches for lower cross section processes. One of the most promising ways to look for MSSM supersymmetry at the Tevatron is associated chargino-neutralino production: $p\bar{p} \rightarrow \tilde{c}_2^0 \tilde{c}_1^+; \tilde{c}_2^0 \rightarrow l\bar{l}\tilde{c}_1^0; \tilde{c}_1^+ \rightarrow l^+ n\tilde{c}_1^0$. This results in a very distinct signature of three leptons and missing energy[4]. Because of its low cross section this search will especially benefit from the increased statistics in Run 2B. The Tevatron's reach in this signature is presented in Figure 3. Note, that Run 2B will not only extend the area of search, but will reach the high m_0 region, which was not accessible before. Good lepton identification is of great importance for this channel.

The supersymmetric partners of top and bottom quarks – *stop and sbottom* - are often predicted to be lighter then other supersymmetric particles[5]. These particles will be produced strongly in $p\bar{p}$ collisions and thus are likely targets for supersymmetric searches. Decay products include b-jets, and searches will require b-tagging. The pseudorapidity distribution of charged tracks produced in decays of these supersymmetric particles is very similar to that of Higgs decay products, as shown in Figure 4 for two distinctly different kinematic cases with very low energy jets in the final state (b) and with very high energy jets (c). In both cases the b-jets fall within the acceptance of the silicon tracker.

Gauge-mediated supersymmetric models predict signatures rich in photons[6]. Interest in these models was sparked by the CDF observation of an $e''e''gg\not{E}_T$ event[7]. Though no other events

have been found, photonic signatures are worth investigating in Run 2B. The phenomenology of extra dimensions also predicts signatures rich in photons[8].

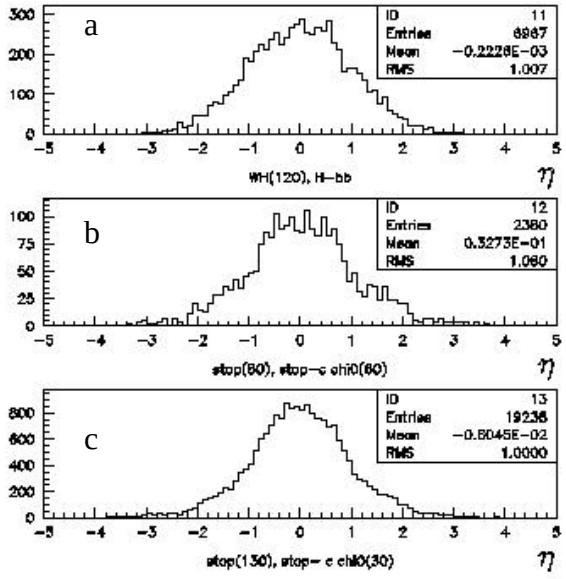

Figure 4 - Pseudorapidity distribution of charged tracks in
a) WH events (M(H)=120GeV/c^2);
b) light supersymmetric top decaying to charm and heavy neutralino
($M(\tilde{t}) = 80GeV/c^2; M(\tilde{c}_1^0) = 60GeV/c^2$*);*
c) heavy supersymmetric top decaying to charm and light neutralino
($M(\tilde{t}) = 130GeV/c^2; M(\tilde{c}_1^0) = 30GeV/c^2$*).*

Alternatives to SUSY are strong dynamics models, for example technicolor or topcolor. Technicolor models predict the existence of technibosons decaying to heavy flavor and gauge bosons[9], e.g. $p\bar{p} \to Wp_T, p_T \to b\bar{b}$. Such searches give vector boson plus heavy-flavor-jets signatures, just like the Higgs search, and will benefit from the detector optimizations motivated by Higgs signatures. More recent topcolor models[10] emphasize non-standard behavior of the top quark and thus could be detected indirectly with thorough studies of top quark properties, or directly through observation of anomalous tb production or production of non-standard Higgs-like bosons decaying to heavy flavor jets.

2.3 Standard Model Physics

These searches for new particles will be complemented by precision measurements of the quanta of the standard model, which provide indirect constraints on new physics, and which will provide the detailed understanding of backgrounds that discoveries will require.

The Tevatron is entering a new era for top quark physics. Greatly increased statistics will be combined, in DØ, with much improved signal sample purity made possible by silicon vertex b-tagging. We anticipate significant improvements in the precision of the top quark mass

measurement, which should reach a level of ~2 GeV with 2 fb^{-1}. The additional statistics of Run 2B should allow this to be pushed down to ~1 GeV. Single top production (through the electroweak coupling of the top) has never been observed. Measurement of the cross section would allow the CKM matrix element $|V_{tb}|$ to be extracted. With $2fb^{-1}$ the cross section can likely be measured at the 20% level, allowing $|V_{tb}|$ to be extracted with a precision of 12%. With $15fb^{-1}$ this uncertainty could be roughly halved. The signatures for top pair and single top production involve vector bosons and heavy flavor jets, just like the SM Higgs. They must be understood in detail for the Higgs search and they will benefit from the detector upgrade.

Precision measurements of the properties of the weak boson will continue to be an important part of the Tevatron program. The W-mass precision should reach 30 MeV per experiment with $2fb^{-1}$ and 15-20 MeV may be achievable with 15 fb^{-1} (theoretical uncertainties are a big unknown in this extrapolation). A W-mass measurement δm_W = 20 MeV combined with a top mass measurement δm_t = 2 GeV will be sufficient to constrain the Higgs mass between roughly 0.7 and 1.5 times its central value. For a 100 GeV best fit, the upper limit of 150 GeV would be well within the Tevatron's region of sensitivity. Such a comparison between direct and indirect Higgs mass measurements would be very interesting whether or not a Higgs signal is seen.

Tests of QCD are important at the Tevatron, both as "engineering" measurements and as probes of strong interaction physics. In the former category, measurements of jet production have reached new levels of precision in Run 1 and are forcing a significant overhaul of the parton distribution functions used in hadron colliders, because the errors on these pdf's must henceforth be treated rigorously. Tevatron jet data from Run 2 will likely provide strong constraints on pdf's and will be an important input to the global fits. In the latter category, many QCD processes have relatively low cross sections and will benefit greatly from increased datasets available in Run 2. Examples are jet production at high-x (jet E_T above about 400 GeV) where the behavior of the cross section is still somewhat uncertain; vector boson plus jet processes, which may be used to determine the strong coupling constant; and diphoton production, which is an important background to Higgs searches at the LHC. In Run 1, DØ accumulated about 200 $\gamma\gamma$ candidates. This will increase to 4000 with 2 fb^{-1}, which is still not a huge number, and to 30,000 with $15fb^{-1}$ of integrated luminosity.

While the DØ detector is not strongly optimized for b-physics, it possesses a number of features that allow it to make significant contributions in this area. As one example, the low-p_T muon triggering and $J/\psi \rightarrow ee$ triggers will allow a competitive measurement of sin 2β in $B \rightarrow J/\psi\ K_S$ events. With $2fb^{-1}$, sin 2β could be determined to $\pm$ 0.07; $15fb^{-1}$ would reduce this uncertainty by almost a factor of three. Of course, the b-physics program will have to operate within a trigger menu that is constrained by the need to cover the high p_T physics priorities of the experiment.

2.4 Summary Of Physics Objectives

The Run 2B DØ silicon tracker is optimized for Higgs boson observation in the $110<M_H<180 GeV/c^2$ mass region. A low-mass Higgs boson decays predominantly to $b\bar{b}$, and thus efficient b-tagging is of paramount importance to Higgs boson searches. Higgs channels will also benefit from the lower trigger thresholds that are achievable from the Silicon Track Trigger. Lepton identification, crucial for the intermediate Higgs mass region, emphasizes

efficient tracking of high p_T tracks in a high occupancy environment and the excellent muon system and the electromagnetic calorimeter of the DØ detector. $Ht\bar{t}$ production puts additional, more stringent, constraints on efficient tracking and secondary and tertiary vertex reconstruction.

It is clear that the entire DØ physics menu of searches, top quark physics, electroweak measurements, QCD, and even b-physics, will benefit from Run 2B. The upgraded tracker will ensure efficient tracking in a high occupancy environment and reduced trigger thresholds for all physics, and efficient heavy flavor tagging for states with b and c-quark jets.

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CHAPTER 3 - SILICON DETECTOR DESIGN

3.1 Introduction

The silicon detector project is introduced in this chapter. The design is based on an optimization of the physics performance of the detector while at the same time satisfying various boundary conditions, both external and internal. The external boundary conditions come from the anticipated accelerator performance in Run 2B. Interfacing the new detector within the existing framework, notably the trigger framework, sets internal constraints. Moreover, building on our experience constructing the Run 2A silicon detector, fabrication and assembly methods proposed for the new silicon detector were reevaluated and the strategy adopted for Run 2B should result in a much more efficient construction cycle. The new detector, for example, will employ only single-sided, modern silicon technology. The remainder of this chapter will describe the basic design features of the proposed silicon detector.

3.2 Design Constraints

3.2.1 Tevatron parameters

In Run 2B the running parameters of the Tevatron will change. The accelerator will run with a bunch crossing of 132 ns, with a beam crossing angle. The half crossing angle will be 136 μradian in each plane. This affects the length of the luminous region. The Beams Division has determined the luminosity acceptance for various running conditions as a function of the fiducial length of the tracker. Luminosity acceptance is defined as the fraction of proton-antiproton collisions that falls within a fiducial length centered around the interaction point. Figure 5 shows the results of the studies for 140 x 103 stores optimized for anti-proton stacking rates of 40 x 10^{10}/hr, and 60 x 10^{10}/hr, with initial longitudinal emittances of 2 eV-sec and 3 eV-sec. Initial transverse emittances of 20 and 15 π-mm-mrad for protons and antiprotons have been assumed, respectively. The calculations include the variation of the length of the luminous region over the course of a store. The curves are normalized to full acceptance at a fiducial length of 200mm.

The luminosity acceptance shows a distinct plateau. The length of the detector is chosen to be on the plateau with an adequate margin with regard to the exact location of the interaction point. In the current design the inner layers have a fiducial length of 96 cm.

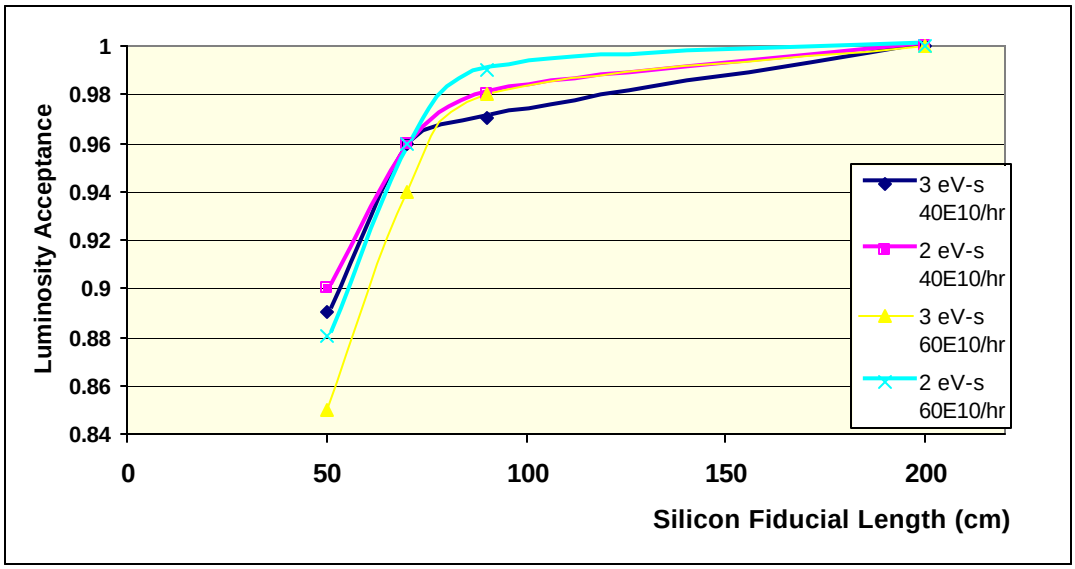

Figure 5 The luminosity acceptance shows a distinct plateau. The length of the detector is chosen to be on the plateau with an adequate margin with regard to the exact location of the interaction point.

3.2.2 Radiation environment

The collaboration embarked on radiation studies of silicon sensors for both the present and proposed Run 2B detector to determine the timescale within which the present detector would become inoperable and to determine the operating parameters for the new detector. The leakage currents and depletion voltages were measured using 8 GeV protons from the booster facility at Fermilab up to a dose of 15 Mrad. The measurements agree with others made outside of DØ and will be described in the next chapter. Based on these measurements, and parameters obtained by other experiments, simulation studies were carried out of the leakage current, depletion voltage, and equivalent noise to determine the silicon operating temperature and to ensure that the device can withstand the foreseen accumulated dose. The design operating temperature of the inner layer was chosen to be –10 degrees Celsius. We also determined that a minimum radius of about 18 mm for the innermost layer of silicon will allow for an adequate safety margin for running the detector to integrated luminosities of 15 fb^{-1}.

3.2.3 Silicon track trigger

The Run 2A silicon detector employs a Silicon Track Trigger (STT) that processes data from the Level 1 Central Track Trigger (CTT) and the silicon tracker. It associates hits in the silicon with tracks found by the Level 1 CTT. These hits are then fit together with the Level 1 CTT information, thus improving the resolution in momentum and impact parameter, and the rejection of fake tracks. The STT has three types of electronics modules:

- The Fiber Road Card (FRC), which receives the data from CTT and fans them out to the other modules.

- The Silicon Trigger Card (STC), which receives the raw data from the silicon tracker front end. It processes the data to find clusters of hit strips that are associated with the tracks found by the CTT. Each card accepts input from at most eight readout hybrids.

- The Track Fit Card (TFC), which fits a trajectory to the CTT tracks and the silicon clusters associated with it. These results are relayed to the Level 2 Central Track Trigger. Each card can accept at most eight STC inputs.

The trigger observes a 6-fold ϕ-symmetry. The STT modules are located in 6 VME crates, each serving two 30-degree azimuthal sectors. Currently each of these crates holds one FRC, nine STCs, and two TFCs - one per 30-degree sector. Each crate can hold at most 12 STCs, with a possibility to go to 16 STC cards with a redesigned backplane. It is these constraints, combined with the 6-fold symmetry that has to be observed, which severely limits the parameter space for the geometry of the silicon tracker.

The data from the silicon tracker must be channeled into the TFC cards such that all hits from a track are contained in one TFC. In layers 0, 1, and 2 overlaps between adjacent sensors are large enough so that each sensor can be uniquely associated with one TFC. This divides the detector into 12 azimuthal sectors. To maintain full acceptance for tracks with p_T>1.5 GeV/c and impact parameter < 2 mm, the data from some sensors in layers 3, 4, and 5 must be channeled into two TFCs, which are in some cases located in different crates. These constraints have resulted in a geometry with 12-fold symmetry for layers 0 through 2, and an 18-, 24- and 30-fold geometry for layers 3, 4 and 5, respectively.

3.2.4 Cable plant

The total number of readout modules in the new system is constrained by the currently available cable plant, which allows for about 940 cables. The present Run 2A detector has 912 readout modules. The cable plant is limited due to space constraints. There simply is not enough space between the central and end calorimeters to route more cables. Only replacing the full cable plant would allow an increase in the number of cables, but this is cost prohibitive. Given that the new detector has more silicon sensors, this implies that not every sensor can be read out and that an adequate ganging scheme will have to be implemented. An elegant solution using double-ended hybrids has been found which is described in the next section.

3.3 Baseline Design Overview

The proposed silicon detector has a 6 layer geometry arranged in a barrel design. The detector will be built in two independent half-modules joined at z=0. The six layers, numbered 0 through 5, are divided in two radial groups. The inner group, consisting of layers 0 and 1, will have axial readout only. Driven by the stringent constraints on cooling, these layers will be grouped into one mechanical unit called the inner barrel. These layers have a significantly reduced radius relative to the current tracker. Given the tight space constraints, emphasis has been placed on

improving the impact parameter resolution. The outer group is comprised of layers 2 through 5. Each outer layer will have axial and stereo readout. The outer layers are also important for providing stand-alone silicon tracking with acceptable momentum resolution in the region $1.7 < |\eta| < 2.0$ where DØ has good muon and electron coverage but lacks coverage in the fiber tracker. The outer layers are assembled in a mechanical unit called the outer barrel. The inner barrel is inserted into the outer barrel forming a half-module. A half-module is the basic unit that is installed in the collision hall. While all 6 layers are designed to withstand 15 fb^{-1} of integrated luminosity with adequate margin, separating the inner layers into a separate radial group provides a path for possible replacement of these layers. The outer layers should easily withstand luminosities up to ~25 fb^{-1}. The inner two layers with axial readout will provide an adequate impact parameter resolution for tagging of b-jets. Two layers as close to the interaction point as possible are preferred to efficiently tag b-jets. The remaining space can accommodate at most four axial-stereo layers, which is adequate to do the pattern recognition. Hence our design calls for six layers.

Of paramount importance to the successful construction of the new detector in the less than 3 years available, is a simple modular design with a minimum number of part types. This is one of the reasons that single-sided silicon sensors are used throughout the detector. Only three types of sensors are foreseen: highly radiation tolerant sensors for layers 0 and 1, with two sizes to best fit the geometrical constraints, and a single sensor size for the four outer layers. All of the sensors are envisioned to have axial traces with intermediate strips. The stereo readout in the outer layers will be accomplished by tilting the sensor slightly with respect to the beam axis.

Figure 6 shows an axial view of the Run 2B silicon tracker. The emphasis is on obtaining improved impact parameter resolution in the R-ϕ plane while maintaining good pattern recognition. The inner two layers have 12-fold crenellated geometry and will be mounted on a carbon fiber lined, carbon foam support structure. Figure 7 shows an axial view of these two inner layers. Layer 0 will have its innermost sensor located at a radius of about 18.6 mm. These sensors will be two-chip wide, 78.4mm long with 50 micron readout pitch and intermediate strips. The pitch is chosen to obtain the best impact parameter resolution possible using conventional technology. Given the size of the luminous region, 6 sensors in z make up one half-module.

Because of the lack of space available and the cooling requirements for the innermost layer, no readout electronics will be mounted on the sensors, i.e. the layer will have 'off-board' electronics. Analog cables will be wirebonded to the sensors, carrying the analog signals to a hybrid where the signals will be digitized and sent to the data acquisition system. Keeping the hybrid mass out of the detector active region also helps in reducing photon conversions. Present CDF experience with noise issues from these cables are a concern but given the requirement that the inner layer has to survive 15 fb^{-1}, there is no alternative to off-board readout electronics. A major challenge in building the mechanical structure for this layer is ensuring that it provides the cooling capability needed to maintain the silicon at a temperature of –10 degrees C while fitting in all the components necessary and keeping mass to a minimum so that the impact parameter resolution is not degraded. The depletion voltages at the end of the run are expected to be around 600V for the innermost layer. The bias system for the inner layers will be designed to deliver voltages up to 1000V.

Layer 1 will contain 3-chip wide sensors that are 78.4mm long with 58 micron readout pitch, with intermediate strips. The geometry matches the segmentation of Layer 0. Because Layer 1 will also sustain substantial radiation doses, the cooling and bias voltage supply requirements will be the same as for Layer 0. Although the heat load from putting hybrids directly on the sensors is greatly increased (0.5 Watts per readout chip), noise and production considerations have led to on-board electronics for all layers except Layer 0.

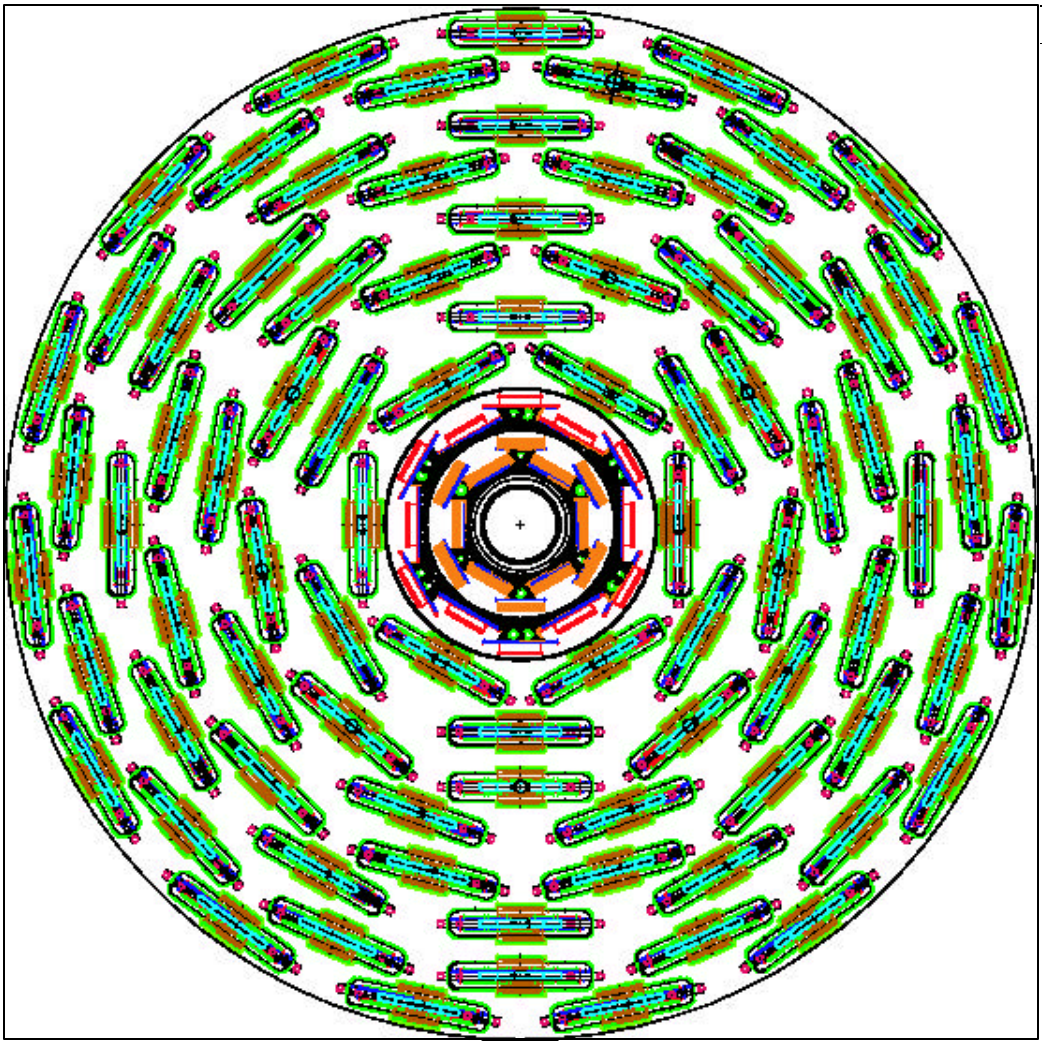

Figure 6 - Axial view of the proposed tracker upgrade. The outer four layers provide both axial and stereo track measurements, while the inner two layers only provide axial track measurements.

In Layers 2-5 only one type of sensor will be used. The sensors will be 5 chips wide, 100mm long with 60 micron readout pitch and intermediate strips. This pitch allows for direct bonding between SVX chips and the sensors and retaining the fine resolution in Layer 5 significantly improves pattern recognition. These layers employ stiff stave support structures. A stave will have carbon fiber sheets mounted on an inner core that will carry the cooling lines. Silicon will

be mounted on the carbon fiber sheets; on one side there will be axial readout and on the other small-angle stereo. The stereo angle will be obtained by rotating the sensors. The design allows for a maximum depletion voltage of 300V for these outer layers. Recall that the detector is built in two halves, a north and a south; each stave will thus cover a half-length in z.

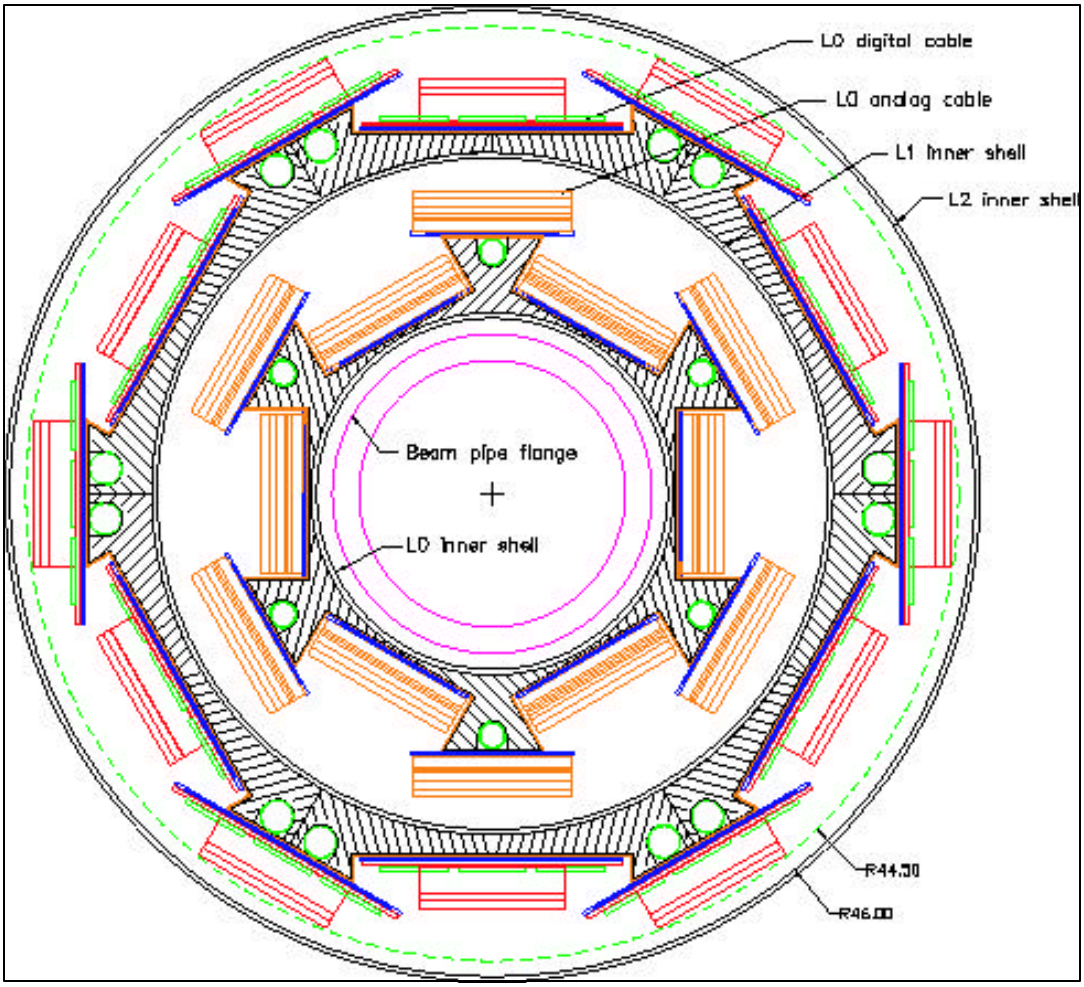

Figure 7- Axial view of Layers 0 and 1 within the sensor active region. The silicon sensors are mounted on a carbon-fiber lined, carbon foam structure with inboard cooling tubes and then are readout using analog low mass cables which connect to hybrids outside of the active region.

The longitudinal segmentation is driven by the need to match η coverage throughout the detector up to η=2. For Layer 1 six sensors, each 78.4mm long, form one half length in z, matching the coverage for L0 which is in the same mechanical structure. For Layers 2 and 3 five sensors, each 100mm long, will form a stave. Staves consist of six 100mm long sensors for Layers 4 and 5. Figure 8 shows a plan view of the tracker inside the fiber tracker.

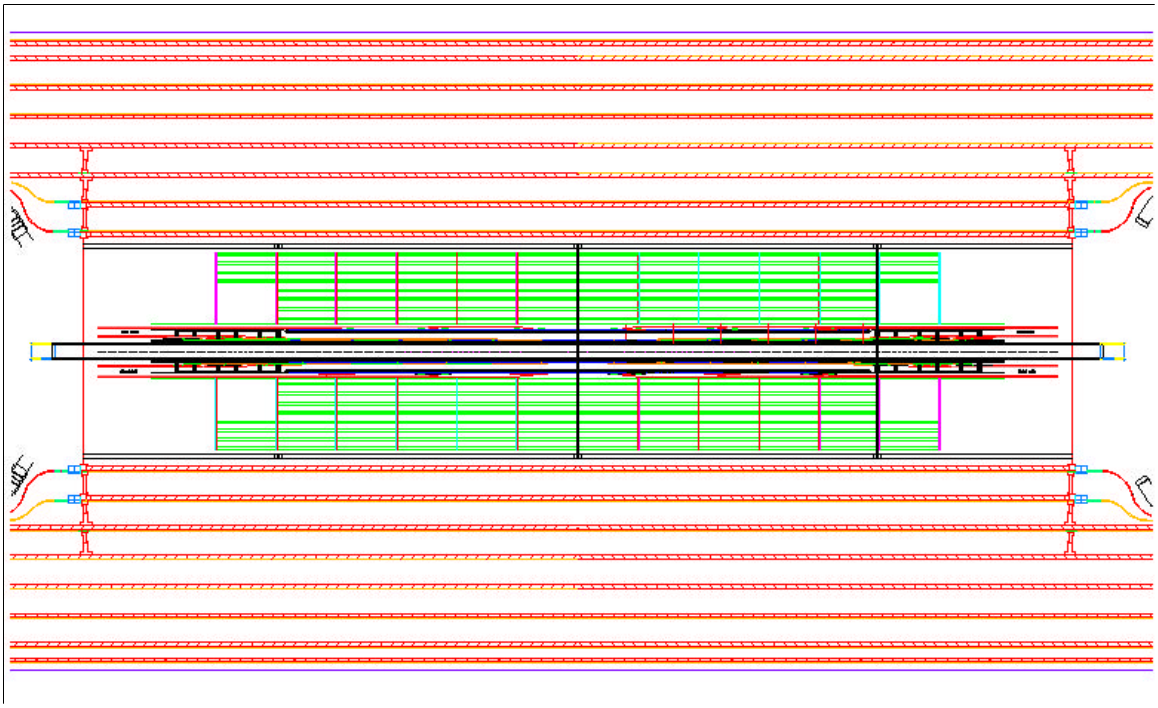

Figure 8 - Plan view of the Run 2B silicon tracker inside of the fiber tracker.

The total number of readout modules in the new system is constrained by the currently available cable plant, which allows for about 940 read outs. The present Run 2A detector has 912 readout modules. This implies that not every one of the 2184 sensors in the detector can be read out separately. By studying deadtime it was determined that for Layers 2 and higher we are able to read out a total of 10 chips. This allows us to use a double-ended hybrid design that reduces the hybrid readout count by a factor of two. A double-ended hybrid services two readout segments at once. Since the sensors are 5-chip wide for the outer layers, the double-ended hybrids will readout 10 chips at a time. The digital signals are carried out of the tracking volume using a digital cable that connects to the hybrid. Layer 1 also employs the double-ended hybrid concept. Since sensors are 3-chip wide in Layer 1, a hybrid will read out 6 chips at a time.

Using double-ended hybrids we've reduced the hybrid count significantly, but not enough to satisfy our cable number constraint. Occupancy studies and confused hit probabilities then determine how best to longitudinally combine (gang) sensors to form a readout segment in z. These are described in DØ Note 3911 [1]. For the inner two layers every sensor is read out separately. For Layers 2 and 3, there are 5 sensors per half-module in z. The two sensors closest to z=0, where the occupancy is highest, are read out individually with one double-ended hybrid. The remaining 3 sensors are connected to another double-ended hybrid. The two sensors at the largest z are wirebonded together and are read out as one unit; the sensor closest to z=0 is read out individually. For Layers 4 and 5 we have a total of 6 sensors per half module in z. Here the two innermost sensors are read out individually as in Layers 2 and 3. The outermost 4 sensors

are ganged together such that each of 2 sensors is wirebonded together to make one readout unit. This arrangement is depicted in Figure 9. Each stave thus has four hybrids, with each hybrid servicing two readout segments, two for the axial readout and two for the stereo readout. The modules are indicated by the length (in cm) of the two readout segments. A hybrid with 10 cm sensors on each side of the hybrid is called a 10/10 module. Similarly there are 10/20 modules and 20/20 modules. Figure 10 shows the longitudinal segmentation for all layers. An 'S' indicates single sensor readout, and '1/2D' indicates a readout segment serviced by one side of a double-ended hybrid. The colors guide the eye to indicate ganged sensors.

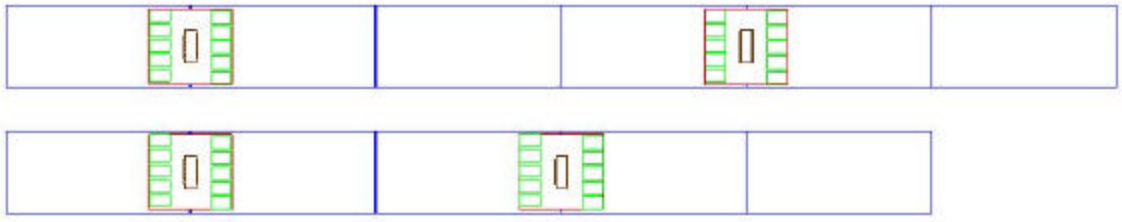

Figure 9 - Readout configuration for outer layer staves. The upper configuration is for layers 4 and 5 and the lower is for layers 2 and 3. Axial readout configuration is shown.

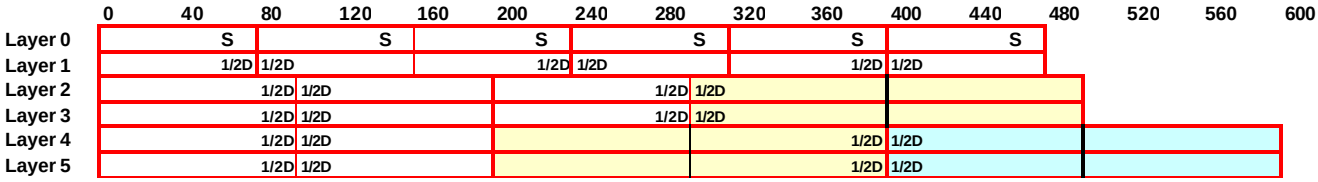

Figure 10 - - shows the longitudinal segmentation of the detector. Here the top row is a ruler showing the length in mm for each of the layers in the detector.

For the stereo side of the stave we have chosen to use the maximum stereo angle possible given the mechanical constraints. This allows us to obtain the best ŕz resolution possible. Studies of confused hits, ghost tracks, and occupancy indicate that it is best for the pattern recognition to have the traces of ganged sensors line up, so as to make one long 20 cm trace. For the 10 cm sides of modules the maximum stereo angle is 2.5 degrees while for the 20 cm sides the maximum stereo angle is 1.25 degrees. We then end up with 6 types of modules for the outer layers: 10/10 Axial and Stereo, 10/20 Axial and Stereo, and 20/20 Axial and Stereo.

The decision was made in November 2000 to read out the new silicon system using the SVX4 chip. Both CDF and DØ will use this chip. This chip is based on the SVX3 chip, but will be produced in 0.25 micron technology. This chip is intrinsically radiation hard and is expected to be able to withstand the radiation doses incurred in the innermost layers. In order not to have to redesign the entire DØ data acquisition and trigger system, the SVX4 chip will be read out in SVX2 mode. The SVX2 chip is the readout chip for the Run 2A detector and incurs deadtime on every readout cycle unlike the SVX3 chip that can run in a deadtimeless mode. As the readout

chip is a joint project with both CDF and DØ, there is a premium on employing the same hybrid technology so that the design work can be shared. We plan to use ceramic hybrids using beryllia. No pitch adapters will be needed in the DØ design so that the SVX4 chips will be wirebonded directly to the silicon sensors for layers 1-5.

The digital signals will be launched onto a jumper cable from the hybrid through an AVX connector. These flex cables will run on top of the stave to a junction card located at the end of the active region on a bulkhead. There will be one junction card per stave. That is, each junction card will service four hybrids, the two hybrids from the axial readout and the two hybrids from the stereo readout. The junction card is a passive element and simply carries the signals from the digital cable to a twisted-pair cable. The twisted-pair cables run to the adapter cards that are mounted on the face of the calorimeter. The adapter card will interface to the existing data acquisition system. The adapter card has two new functions in Run 2B. First, it will convert 5V lines to 2.5V, necessary for operating the SVX4 chip. The current data acquisition system uses the SVX2 chip, in which the lines are single-ended. The SVX4 chip will be run differentially at 2.5V. The adapter cards will convert the single-ended lines to double-ended lines. From the adapter card downstream, it is anticipated that we can retain the full data acquisition system as is. Some modifications will be needed for the interface boards that pass the voltages to the detector to allow for higher voltages for the biases for the inner layers, but no major modifications are foreseen.

The design parameters are summarized in Table 1. There are a total of 2184 silicon sensors in this design, read out with 888 hybrids containing 7440 SVX4 chips. In layers 2-5 there will be a total of 168 staves, containing 336 readout modules. For comparison, the Run 2A silicon detector has 793K readout channels while the Run 2B one will have 952K readout channels. The Run 2B silicon detector is designed to allow for faster construction due to fewer and simpler parts than the Run 2A device. Comparisons between the detectors show that the major difference between the two detectors is found at the inner and outer radii. Figure 11 shows axial views of both detectors drawn to scale. By decreasing the radius of the innermost layer from 25.7 mm to 18.6 mm, the impact parameter resolution is cut by a factor of 1.5. Because we are removing the F-disks and the entire cable plant from the Run 2A barrel modules, we are able to utilize this space at larger radii for silicon sensors. The increase from 94.3mm to 163.6mm for the outer radius allows us to put in two more layers of tracking necessary for the pattern recognition in the Run 2B environment. With the new detector we will have better stand-alone silicon tracking. A number of factors affect the tracker performance, and consequently the physics performance, of the detector. Among these factors are tracker acceptance, amount of material, resolution, and pattern recognition capabilities. We have optimized our design to the extent possible to obtain a detector that is superior to the Run 2A detector and that will allow us to be well placed for the possibility of discovering new physics.

Table 1 - Design Parameters. There are a total of 2184 sensors and 888 hybrids in this design.

Layer	Nphi	R (mm) Axial	R (mm) Stereo	# Sensors in z	# Sensors Total	Sensor Width (mm)	Readout Pitch (μm)	# Readout in z	# Chips per Readout	Total Chips	# Hybrids Total
0A	12	18.55	---	12	72	15.50	50	12	2	144	72
0B	12	24.80	---	12	72	15.50	50	12	2	144	72
1A	12	34.80	---	12	72	24.97	58	12	3	216	36
1B	12	39.00	---	12	72	24.97	58	12	3	216	36
2A	12	53.23	56.33	10	120	41.10	60	8	5	480	48
2B	12	68.93	72.03	10	120	41.10	60	8	5	480	48
3A	18	89.31	86.22	10	180	41.10	60	8	5	720	72
3B	18	103.38	100.28	10	180	41.10	60	8	5	720	72
4A	24	116.91	120.00	12	288	41.10	60	8	5	960	96
4B	24	130.58	133.67	12	288	41.10	60	8	5	960	96
5A	30	150.08	146.99	12	360	41.10	60	8	5	1200	120
5B	30	163.59	160.49	12	360	41.10	60	8	5	1200	120
Total					**2184**					**7440**	**888**

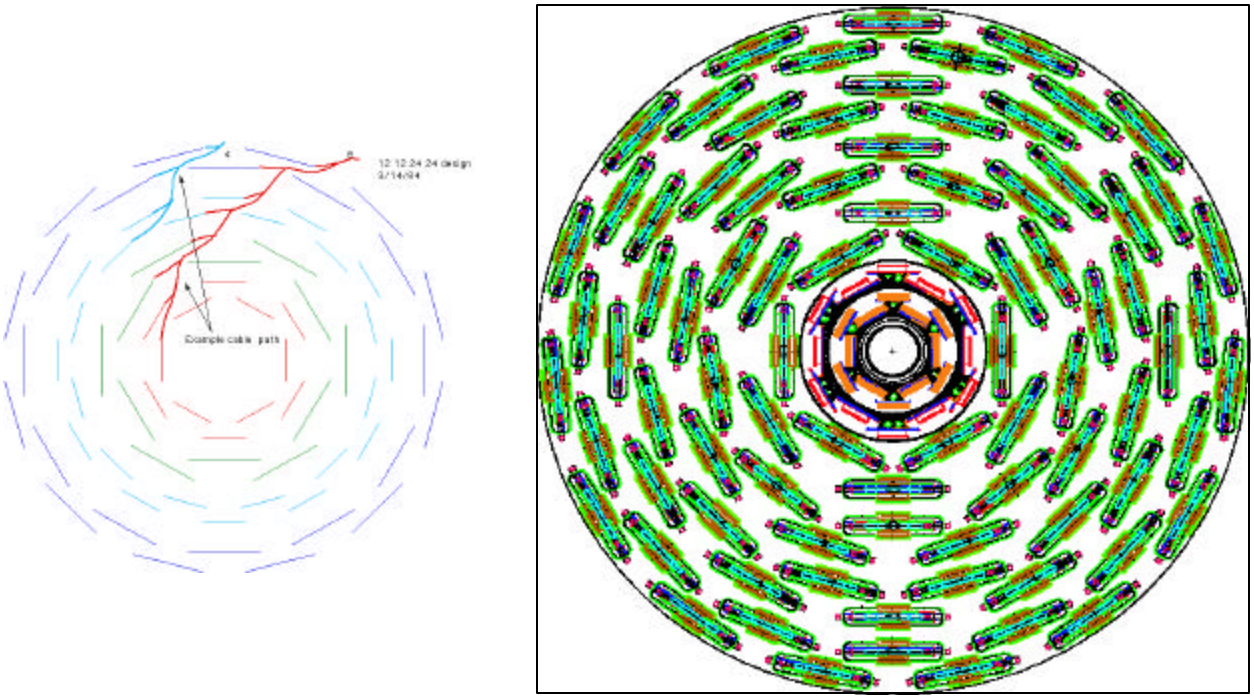

Figure 11 - Comparison of the axial views of the Run 2A and Run 2B silicon detectors. The left picture shows the Run 2A detector whose innermost layer resides at a radius of 25.7mm. The innermost layer of the Run 2B detector resides at a radius of 18.5 mm.

[1] DØ Note 3911, "MCFAST Studies of the Run2b Silicon Tracker", R. Lipton and L. Stutte, October 4, 2001.

CHAPTER 4 - SILICON SENSORS

4.1 Introduction

The main requirements for the silicon detector is efficient and reliable tracking, precise vertex measurement, and radiation hardness. As described above, this is achieved with a 6-layer device. The four outer layers are constructed of 60 μm pitch silicon sensors and provide hits essential for pattern recognition in a high-occupancy environment. In addition, two inner layers 0/1, constructed with 50/58 μm pitch silicon sensors with intermediate strips at 25/29 μm, provide precise coordinate measurement essential for good secondary vertex separation. Reliable operation of silicon sensors in a high-radiation environment is critical to the experiment's success. Over the operating period, the inner layers of the Run 2B silicon detector will be subject to a fluence of about 2×10^{14} equivalent 1 MeV neutrons per cm^2. We were guided in our design and technology choice by our experience in Run 2A detector construction as well as by recent research and development in the radiation hard technology.

4.1.1 Lessons from Run 2A

Several difficulties were encountered by DØ during the Run 2A silicon detector prototyping and construction. The gained Run 2A experiences and important conclusions are listed in the following:

- Sophisticated double-sided silicon sensors were difficult to produce and lead to lower yield and hence significant delays. Single-sided sensors however, which have been produced both by Elma for the H-disks and Micron for the 1st and 3rd layers of barrels 1 and 6 for the Run 2A detector, had higher yields and caused much less trouble due to their simplicity.

- The introduction of an alternative vendor at the later stages helped to speed up production.

- The large number of sensor types complicated the production process.

- Double-sided sensors proved to be very difficult to handle.

- Radiation studies have shown that double-sided (and especially 90^o double-metal) silicon sensors have limited radiation hardness (more details in "Radiation testing")

- Detailed pattern recognition studies have shown that in high occupancy environment, "ghost" hits produced in 90^o sensors lead to a significant fraction of fake tracks and increased reconstruction time.

For Run 2B silicon sensors, we adopted the following guidelines:

- Use only single sided silicon sensors.

- Try to identify alternative vendors whenever possible.
- Limit the number of sensor types to 3.
- Use only small stereo angles, achieved by sensor rotation.
- Avoid double metalization.

In our choice of radiation hard technology we have benefited greatly from radiation hard silicon R&D studies motivated primarily by the needs of LHC experiments.

4.1.2 Radiation damage in silicon

The most important damage mechanism in silicon is the bulk damage due to the non-ionizing part of the energy loss, which leads to a displacement of the silicon atoms in their lattice. It causes changes in doping concentration (and, eventually, silicon type inversion), increased leakage current, and decreased charge collection efficiency. Surface damage due to ionizing radiation results in charge trapping at the surface interfaces and leads to increased interstrip capacitance and, therefore, electronics noise.

The increase in bulk leakage currents after radiation exposure is caused by additional generation of electron-hole pairs. For the operation of detectors the control of leakage current is important in two aspects, one is the resulting higher shot noise, the other is the increased bulk heat production in silicon which may lead to a thermal runaway if the silicon detector is not properly cooled. The bias leakage current increase is directly proportional to the active strip volume of the silicon detector and to the particle fluence the detector is exposed to. It neither depends on the chosen silicon material or technology, nor on the exact manufacturing of the detector. However, the currents scale down considerably with the temperature. Cooling the detectors to 0^{o} C typically reduces the leakage current to 1/6 of its value at room temperature.

The change in the effective doping concentration measured as a function of the particle fluence for n-type starting material shows a decrease until the donor concentration equals the acceptor concentration or until the depletion voltage is almost zero, indicating intrinsic material. Towards higher fluences the effective concentration starts to increase again and shows a linear rise of acceptor-like defects. Many experimental groups have confirmed this phenomenon of changing from n-type to p-type like material and usually the detector is said to have undergone a type-inversion from n-type to p-type. The radiation-induced changes of the doping concentration are initially not stable and exhibit two main components with different time behaviors and temperature dependences. With time constants in the range of a few days a decrease in the radiation induced changes occurs soon after irradiation. This effect is called short-term annealing or beneficial annealing, because it mitigates the acceptor creation and hence the type inversion process. However, at room temperature an increase in the acceptor states appears after about two weeks of annealing leading to even higher depletion voltages. This long term or reverse annealing is a major concern because of its limiting factor for long-term operation of silicon detectors in high fluence regions. Reverse annealing can be almost completely suppressed by cooling the detector to -5^{o}C or less and by minimizing the maintenance periods of the silicon detectors at room temperature.

The third effect is the reduced charge collection efficiency. The primary mechanism leading to a decrease in the collection of electrons or holes is charge trapping at defect sites, i.e. a decrease of the carrier lifetime with increasing fluence. In addition surface damage in the silicon oxide due to ionizing radiation results in the creation of fixed positive charge at the surface boundary between silicon and silicon oxide. This leads to increased interstrip capacitances and, therefore, higher electronic noise.

Seriously damaged detectors will require high bias voltages to operate efficiently. The deteriorated charge collection can be efficiently recovered by applying a bias exceeding the depletion voltage. This overbiasing also reduces to normal values the increased interstrip capacitance due to the surface charge accumulation. So the high voltage operation is crucial for radiation hard silicon and at the end the breakdown voltage of the device will determine the limits of survivability.

4.1.3 Radiation hard designs

The CMS collaboration designed single-sided 300 μm thick n-type sensors, which were reliably working after heavy irradiation at bias voltages up to 500 V[1]. The main features of the design are p+ strips in n-bulk silicon, which are biased with polysilicon resistors and are AC coupled to the readout electronics. The front side of the detector (with p+ strips) has a peripheral n+ implantation (n-well) at the edge and is followed by a p+ single guard ring structure to prevent junction breakdowns. This guard ring design has been optimized in cooperation with Hamamatsu and is also successfully implemented with other producers. It is proven to be radiation hard and CDF is using this type of sensors for the L00 of SVX in Run 2A. Other radiation hard designs reduce the risk of an early breakdown at the edges of the silicon by including a multi-guard ring structure[2].

We note here that in the case of AC-coupled double-sided sensors (as presently used by CDF and DØ in Run 2A) the high bias voltage is applied across the coupling capacitor on one of the sides (unless the electronics is floating at the same potential). Together with considerably higher costs related to the double-sided wafer processing, the requirement that AC capacitors hold off the bias voltage is a strong limitation for the double-sided detectors and we are not considering using them for the upgrade.

One of the main methods for improving the radiation hardness is the use of low-resistivity silicon as an initial detector material[3]. Low bulk resistivity of silicon corresponds to high depletion voltage of the device. For example, a 300-micron thick detector with bulk resistivity of $r \approx 1.0 k\Omega \cdot cm$ depletes at $V_{depl} \approx 300$ V. High initial depletion voltage values shift the type-inversion point to higher fluences, which limits the depletion voltage growth after the type inversion, thus improving the radiation hardness of the sensor.

A new technological development driven by the R&D work of the ROSE collaboration[4] uses oxygenated silicon materials to improve the radiation hardness of silicon detectors. Oxygen concentrations ($[O_i] \approx 10^{17} cm^{-3}$) in silicon improve considerably the radiation hardness of the detector for charged particle fluence and effectively lower the needed bias voltage for radiation damaged detectors. No improvement was observed for damage caused by neutrons. The

charged particle component is expected to dominate (for example at CMS only $1/10^{th}$ of the damage is accounted for by neutrons). There are indications also that the reverse annealing saturates at high fluences for oxygen enriched silicon.

High oxygen concentrations reduce the donor (n-impurity) removal rate significantly and can mitigate the acceptor (p-impurity) creation. The simplest way to enrich silicon material with oxygen is a diffusion process in the $\sim 1200^{o}C$ oxygen atmosphere of a quartz oven. This technology is easy and economic and has been successfully transferred to a number of silicon detector vendors.

Finally there is an alternative to use n+ strips on n type silicon. It has been shown that they offer a better collection efficiency at under-depleted voltages and, therefore, would improve the performance after irradiation. However, the detectors technologically are more complicated and require further R&D efforts. Since for $n^{+}n$ sensors certain techniques like p-stop or p-spray are necessary to maintain the strip isolation, the detectors are becoming more and more complex which would considerably drive up the costs. Furthermore, it is not clear that such a fine pitch structure of 25µm we are requiring for layer 0 is technologically feasible on $n^{+}n$ devices. Except LHCb, which is pursuing a $n^{+}n$ option for its vertex microstrip detector, neither of the other LHC silicon strip detectors will use $n^{+}n$ and we are considering this technology as too risky for the tight Run 2B schedule.

In summary, two approaches have been successfully explored so far:

- Low-resistivity silicon sensors. Increasing initial donor concentration leads to type inversion after higher radiation doses, thus slowing the radiation damage.

- Oxygenated silicon. Controlled increase in oxygen concentration slows down the growth of depletion voltage with irradiation dose.

It is possible to combine both approaches. Both techniques have been transferred to multiple silicon vendors.

4.2 Silicon Sensors For Run 2B

4.2.1 Technology choice for Run 2B DØ SMT

For the construction of the Silicon Microstrip Tracker for Run 2B DØ we propose the use of AC-coupled, single-sided single-metal p^{+} on n-bulk silicon devices with integrated polysilicon resistors as baseline sensors. Only bias resistors based on polysilicon are capable of sustaining the high radiation level the Run 2B detector will experience. Either a multiguard structure (see Figure 12 a) or a single guard ring structure with a peripheral n-well at the scribing edge (see Figure 12 b), developed in cooperation with Hamamatsu's design engineers, is necessary to allow operation at high bias voltages.

a) b)

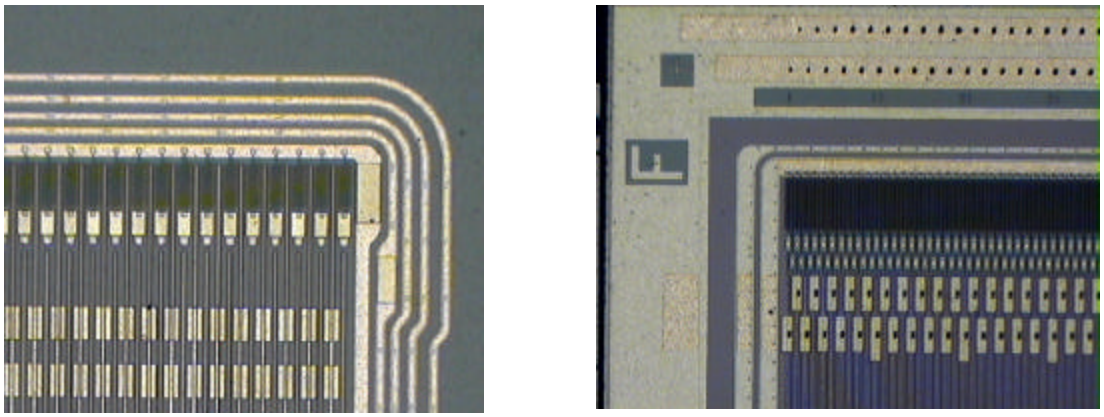

Figure 12. - a) Multiguard ring structure of ELMA prototype sensors. b) Hamamatsu's sensor with a single guard ring structure and a peripheral n-well.

We prefer a silicon microstrip vendor capable of doing multilayered dielectric substrates for the coupling capacitors for mainly two reasons. First of all, it will significantly reduce the number of developing pinholes and therefore shorted capacitors in the detector. Secondly, by using silicon nitride (Si_3N_4) in addition to silicon oxide, the coupling capacitor value can be increased while leaving the thickness of the dielectric substrate constant.

Oxygenation is considered as a serious option for the inner layers 0 and 1 in order to improve the radiation hardness further.

4.2.2 Sensor geometry

DØ envisions using 3 sensor types for Run 2B. Their geometric parameters are summarized in Table 2.

Table 2. - Geometric parameters of silicon sensors.

Layers	Length (mm)	Width (mm)	Strip pitch /readout pitch (μm)	# readout channels	# of sensors + spares
0	78.4	14.8	25/50	256	144+50%=216
1	78.4	24.3	29/58	384	144+50%=216
2-5	100.0	41.1	30/60	640	1896+20%=2280

All outer layers are constructed from sensors of the same type. In the specified geometry, two such sensors can fit on one 6" silicon wafer. Unfortunately, 6" technology is not widely used among silicon sensor manufacturers, with only Hamamatsu and Micron Semiconductors having implemented it successfully so far. Other vendors continue producing sensors using 4"

technology. It is possible to modify the design to use two 50-mm long sensors, which can fit on a 4" wafer, instead of one 100-mm long sensor. This choice has drawbacks: increased number of parts; additional wire-bonding load; increased dead area; and, most importantly, significant increase in cost.

We chose to use sensors 78.4 mm long for layers 1 and 0 to minimize occupancy and noise, and more importantly, to take advantage of a wider choice of vendors. These sensors can be fabricated with two L0 type sensors or one L1 type sensor on a single 4" wafer. Since these sensors will be subject to a very harsh radiation environment, it is critical to choose a vendor that can provide radiation-resilient devices.

We plan to use intermediate strips in all sensors to improve the single hit resolution. A multiple guard-ring, or Hamamatsu-style guard-ring, structure is necessary to ensure high breakdown voltage. This structure occupies 1-mm wide area on each edge of a silicon sensor.

4.3 Radiation Environment And Sensor Performance

Performance of silicon sensors depends on factors such as irradiation dose, operating temperature, and duration of shutdowns.

We use the following estimates for the charged particle and neutron fluences [5]:

$$\Phi_{ch} = \frac{1.175 \cdot 10^{11}}{r^2} cm^{-2} / pb^{-1}$$

$$\Phi_{n} = 1.8 \cdot 10^{9} cm^{-2} / pb^{-1}$$

where r is the perpendicular distance to the beam line in cm. The charged particle fluence was assumed to be composed of 64% pions and 36% protons.

An independent study of particle fluences in DØ was also carried out in ref. 6 based on a simulation employing the DTUJET event generator and a GEANT/CALOR simulation of the DØ detector, hadronic interactions, and secondary particle production. In comparison with the fluences used here, ref. 6 found a similar neutron fluence, but found a charged particle fluence about a factor of two lower. However, to be conservative, we do not reduce our charged-fluence estimate. We assume 2.8 fb^{-1} of integrated luminosity in the first year of operation and 4 fb^{-1} in each of the following years[7].

Operating temperature is another important factor affecting the detector performance in the high radiation environment. The choice of operating temperature depends on detector characteristics, electronics design, and mechanical and cooling constraints. Operating the detector near its room temperature assembly environment minimizes mechanical stresses. Very low temperature operation implies exotic coolants and/or large cooling passages as well as good thermal contact everywhere. The final choice of –10 degree C operating temperature is a compromise between detector operating voltage, signal to noise ratio, and mechanical and cooling constraints.

We also assume a 4-week maintenance period at room temperature at the end of each year. Detector annealing and radiation damage parameters are taken from Rose collaboration data[4].

The resulting depletion voltage as a function of operating temperature for the layer 0 sensors is shown in Figure 13.

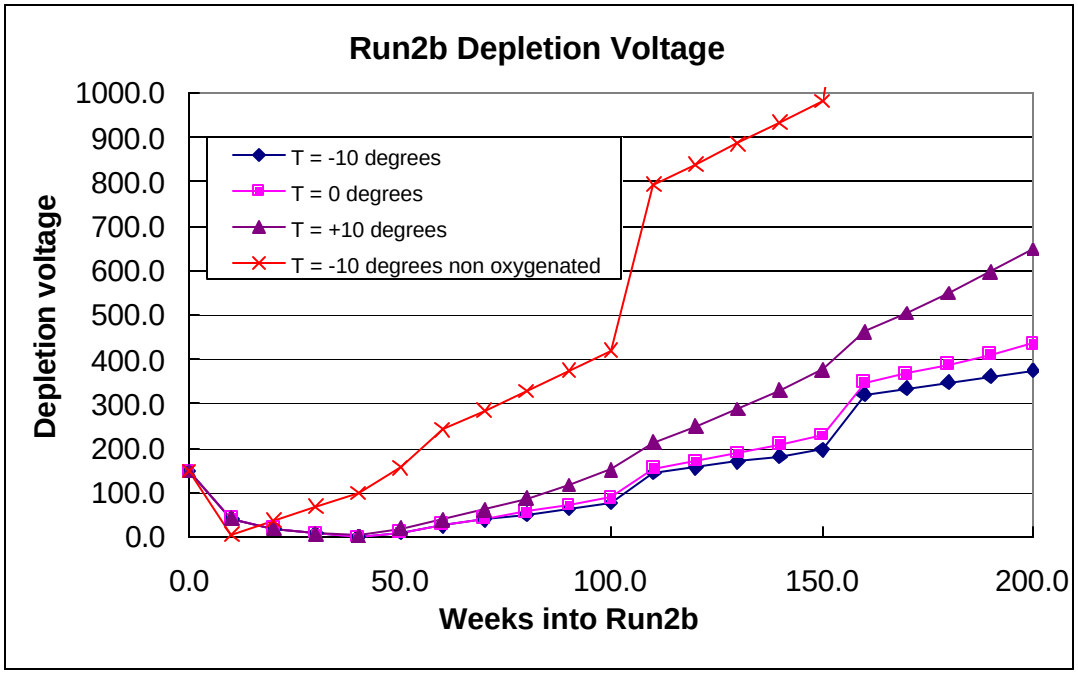

Figure 13. - Depletion voltage for layer 0 sensors as a function of weeks in Run 2B. Two hundred weeks corresponds to an integrated luminosity of 14.6 fb-1 and a dose of 15 Mrad.

Temperature effects of reverse annealing tend to saturate below –5 degrees C and increase rapidly above +10 degrees C. It is quite important to keep the maintenance periods to a minimum. There is a wide variation in reverse annealing parameters among manufacturers who do not use oxygenated silicon. We feel that it is important to irradiate samples of detectors used in Run 2B to verify that the damage response is consistent with operation to 15 Mrad. The inner layer detectors will be specified to operate at 700 V. Operating the inner layer below –5 degrees will give us adequate operating voltage performance for detectors with reverse annealing characteristics of oxygenated silicon. Our –10 degree C design should accommodate production variations among sensors and provide a reasonable operating margin.

For the outer layers we hope to minimize the mass and simplify the design of the bias circuitry by limiting the operating voltage of these layers to ~300 V. Figure 14 indicates that depletion voltage performance at or below –5 degrees C is satisfactory for all layers with oxygenated silicon and for layers 2-5 (R>5cm) for any silicon variety.

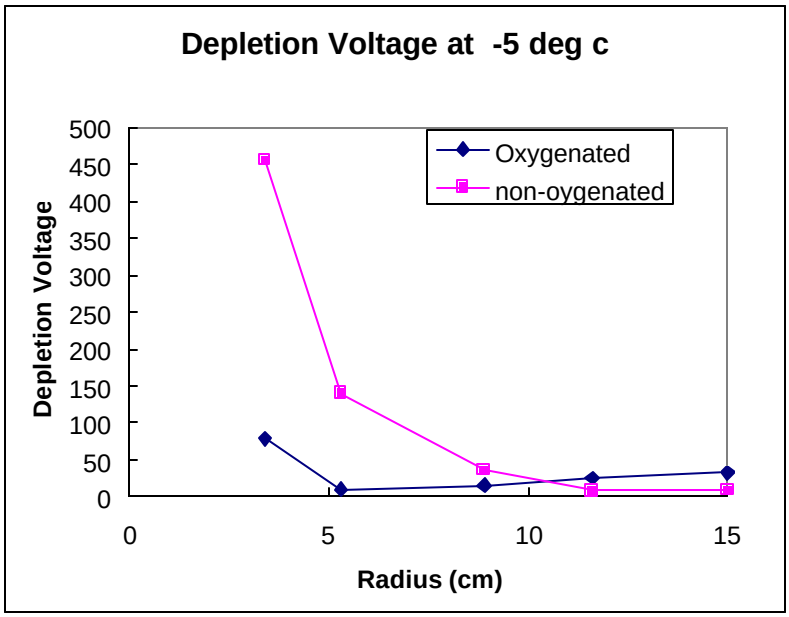

Figure 14. - Depletion voltage as a function of radial position.

According to these estimates layer 1 and the outer-layer sensors will be able to easily withstand a radiation dose equivalent to 20 fb^{-1}. The depletion voltage in layer 0 sensors is expected to reach 600V after 15 fb^{-1}. As we pointed out earlier, oxygenation is essential to slow down the depletion voltage growth after type inversion occurs. In addition, reduced temperature during maintenance periods will provide significantly greater longevity.

Signal to noise ratio (S/N) is an important parameter that ultimately limits the detector lifetime. Based on previous studies and CDF experience in Run 1, S/N starts affecting b-tagging efficiency when it goes below 5 [8]. Our design goal is to keep the S/N above 10.

In our signal-to-noise (S/N) estimates we assume that sensors can be fully depleted and that one MIP produces 23,000 $\bar{e}$ in 300 μm silicon. We have considered several contributions to the total noise:

- Noise due to load capacitance of the analog cable (0.35 pF/cm) and detector (1.2 pF/cm), parameterized as 450+43C(pF/cm) based on SVX4 chip specifications.
- Noise due to the series resistance of the analog cable
- Shot noise from detector leakage current
- Thermal noise due to the finite value of the bias resistor (~200e^-).

Shot noise and series noise are temperature dependent and can be minimized by running at low temperature. Figure 15 shows the total noise for layer 0 sensors as a function of temperature for various lengths of analog flex cable. Operation below –5 degrees C provides satisfactory

performance. Design for –10 degree C operation will provide operational margin if thermal contacts or coolant flows are not as expected.

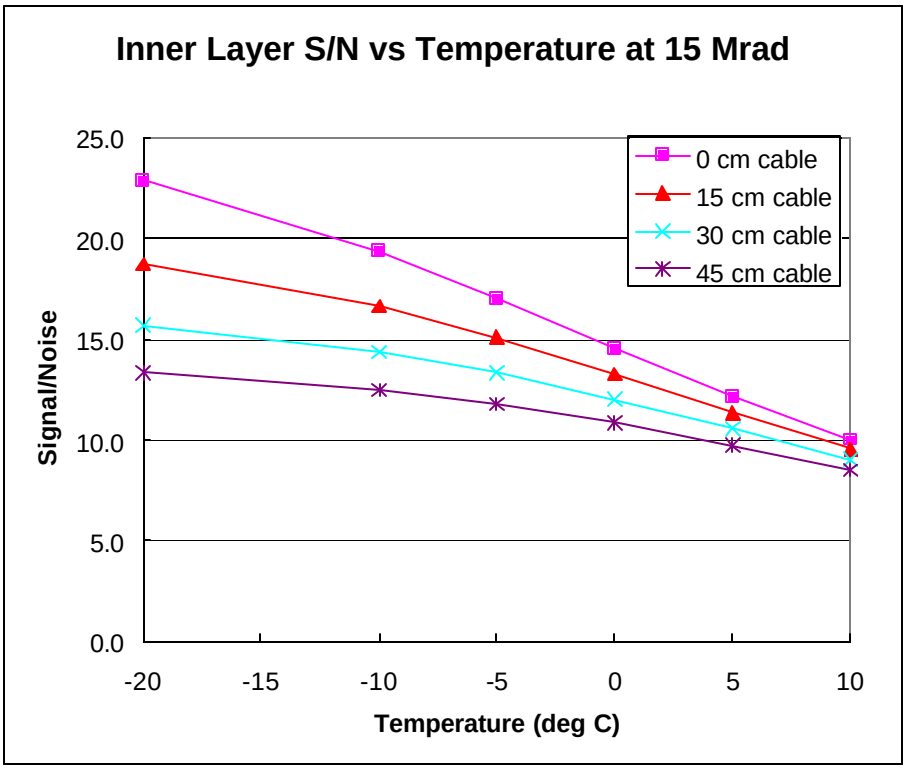

Figure 15. - Inner layer signal/noise ratio as a function of operating temperature for various analog cable lengths.

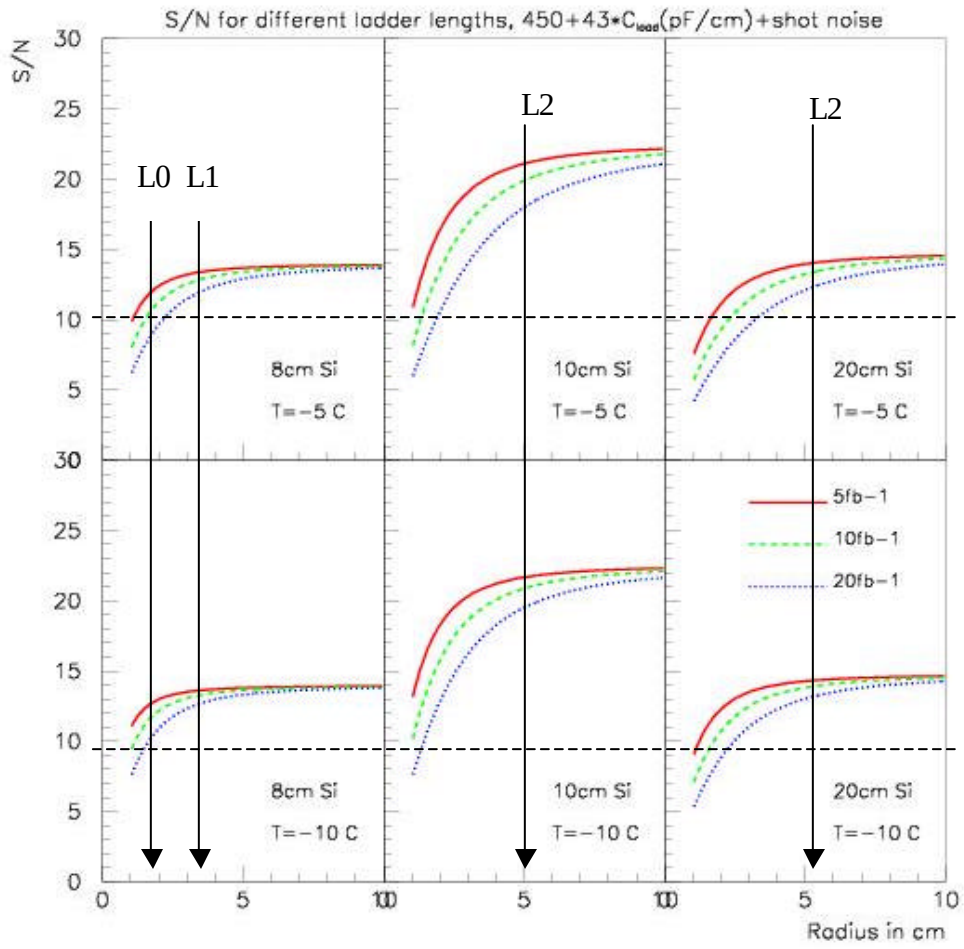

Figure 16. - Signal to noise ratio as a function of radius for different running temperatures and sensor length. In each plot, the solid curve corresponds to exposures of 5 fb^{-1}, dashed – to 10 fb^{-1} and dotted - to 20 fb^{-1}.

Figure 16 shows S/N behavior as a function of radial position of the sensors. For 8 cm long sensors used in layers 0 and 1, the S/N is greater than 10 after 20 fb^{-1}, if the running temperature is below -5^{o}C. In layers 2 through 5 modules are constructed of one or two 10 cm long sensors. Modules with one sensor provide very robust S/N above 15. For two-sensor long modules (20 cm) the S/N can be kept above 10.

In summary, based on our estimations of depletion voltage and S/N we have sufficient safety margin in Run 2B. To verify our predictions we have tested silicon sensors from several potential Run 2B vendors at the RDF facility in the Fermilab Booster.

4.4 Radiation Testing Of Silicon Sensors

4.4.1 RDF

Radiation tests described here were carried out at the RDF facility in the Fermilab Booster. The facility provides 8 GeV protons for various irradiation studies. The beam is ~0.5 mm in radius and is typically $>3x10^{11}$ protons per pulse, with a typical repetition rate of one pulse/3 sec. Beam flux is measured by a toroid and confirmed by irradiation of aluminum foils. Detectors are mounted in a cold box, which maintains detector temperature at 5 degree C and allows for detector bias and monitoring. The box is in turn mounted on a x-y table which scans the detector assembly through the beam; insuring uniform irradiation.

Irradiation typically takes one shift. This intense irradiation can leave a substantial charge in the oxide and on detector surfaces. Detectors are then left at 5 degrees C to "cool down" and anneal for ~1 week before testing.

4.4.2 Run 2A detector irradiation studies

To understand the expected lifetime of the Run 2A detector we performed a series of measurements with spare or grade B modules. We used 3 different ladder/wedge types of double-sided detectors and one type of single sided detector. All detectors are processed on n-type bulk silicon material with a typical thickness of 300μm with integrated AC coupling and polysilicon bias resistors. The double-sided ladders had either 6, 9 or 14 readout chips on the their front end hybrid, which was directly glued on the silicon. The 6-chip detector is manufactured on a 6''-wafer technology and has 90° stereo strips on the n-side. The 9-chip detector is a stereo detector with a small angle view of 2°. The 14-chip module is a double-sided wedge-shaped detector with varying strip length and angle of ±15° on both sides.

The lifetime of the Run 2A detectors is likely to be determined by the limited voltage that can be applied across the AC coupling capacitors. These capacitors break down near 150 V and can only be safely operated to ~100 V. Thus, with split bias we expect to be limited to a total bias of 200 V. In addition during ladder testing we found that the Micron detectors are subject to microdischarge breakdown on the junction side. The breakdown voltage varies on a detector-to-detector basis but can limit the junction side bias to as low as 10 V. This effect switches sides upon type inversion and is partially mitigated on the n side by compensating effects of oxide charge.

In order to characterize the performance of the irradiated detectors and to understand their behavior after irradiation the following measurements have been carried out:

- leakage current measurements
- depletion voltage determination
- average noise determination
- number of noisy channels

Depletion voltage was measured by measuring the response to a 1064 nm laser, noise and current measurements were performed using our standard set of detector burn-in tests.

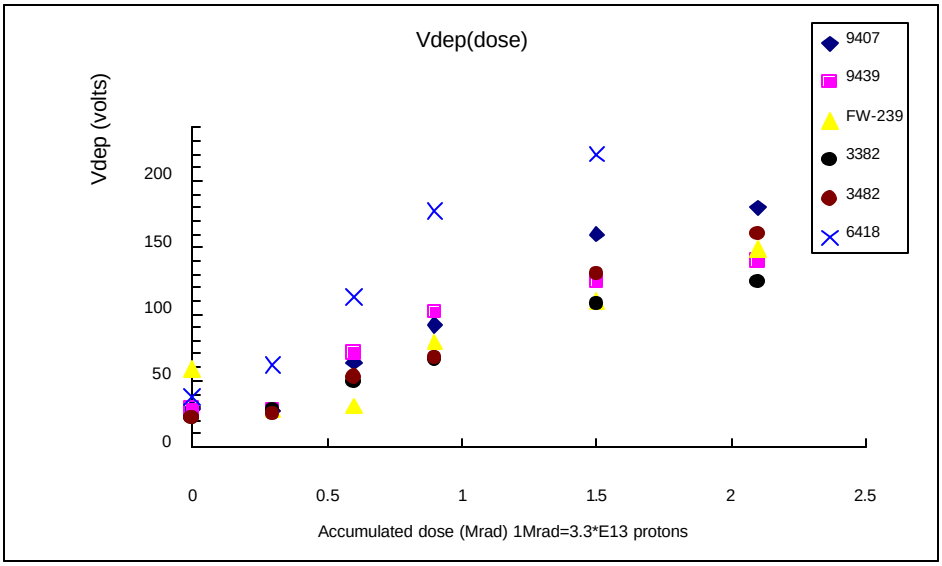

Figure 17. - Depletion voltage as a function of accumulated dose. Detector types 9xxx-layers 2,4; FWxxx-F wedge; 3xxx layers 1,3 barrels 1 and 6 (single sided); 6xxx – layers 1 and 3 barrels 2-5 (double sided double metal)

Figure 17 shows our results for depletion voltage. With the exception of the double sided double metal (DSDM) devices all detectors perform as expected. The DSDM detectors seem to have a depletion voltage at 1.5 Mrad almost a factor of two higher than other devices. Since these detectors are at the inner radius of the silicon detector they will limit the lifetime of the tracker. The cause of this effect is not understood. All detectors were exposed at the same time and tested with identical setups. It is possible that the DSDM detectors are more susceptible to surface charge than simpler devices. We are planning to perform an additional irradiation with test structures to try to understand if this effect is due to bulk silicon properties or an effect of the fabrication.

Figure 18 and Figure 19 show the noise in the ladders as a function of dose as measured in the burn-in test at 3 deg C. The most probable pulse height for a MIP is ~26 ADC counts. The contribution from shot noise is ~0.8 ADC counts at 2.1 Mrad. In general the noise rises from 1.5-2.0 counts to ~3 counts, giving a worst-case signal/noise ratio of 9:1. The DSDM detector (6418) has additional noise which rises to 5 counts on the n-side at 2.1 Mrad. This is due to the onset of microdischarge on the n side of this ladder.

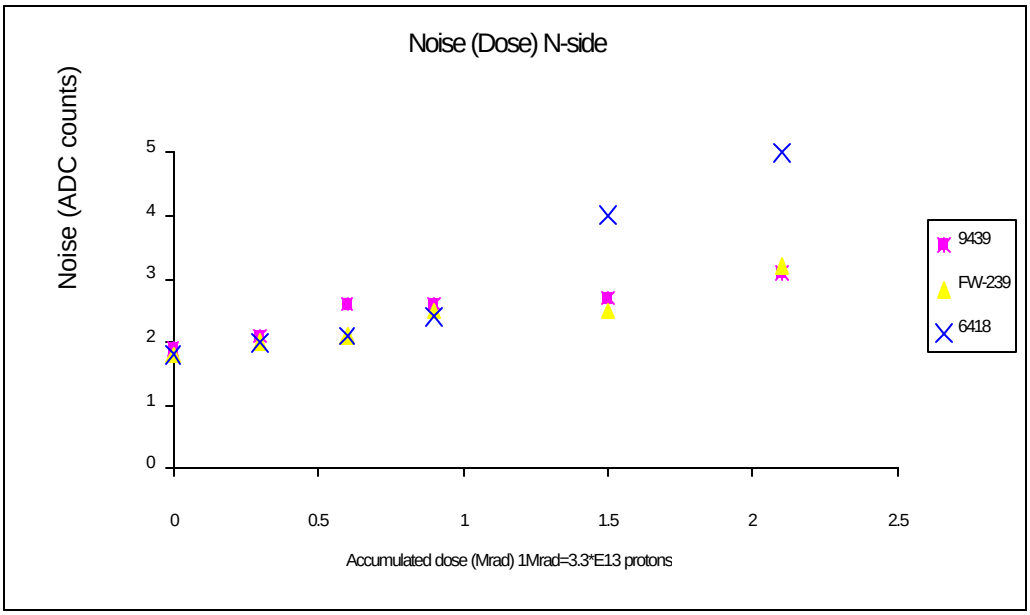

Figure 18 Noise in n-side of Run 2A ladders as a function of radiation dose.

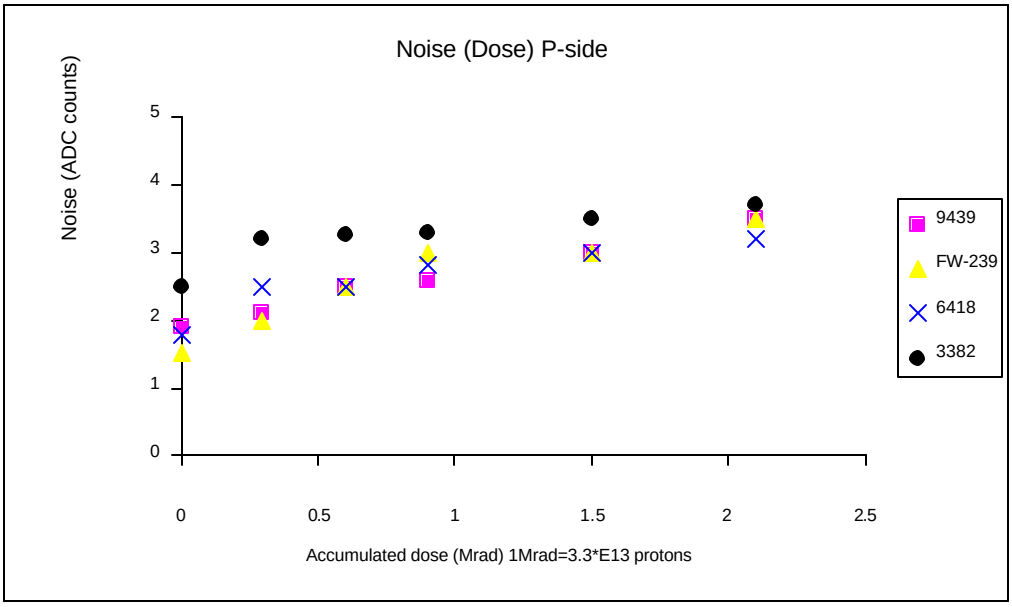

Figure 19. - Noise in p-side of Run 2A ladders as a function of radiation dose.

4.4.3 Run 2B detector irradiation studies

We have performed a set of irradiation studies on single sided detectors of the type to be used for Run 2B. The detectors used were either CDF layer 00 devices (Hamamatsu, Micron, ST) or prototypes specifically for DØ (ELMA). Two Micron detectors were oxygenated, the ELMA devices were also oxygenated, but at a level too low to affect the depletion voltage. These detectors were exposed to 5, 10 and 15 Mrad doses. We measured depletion voltage and leakage current after each exposure.

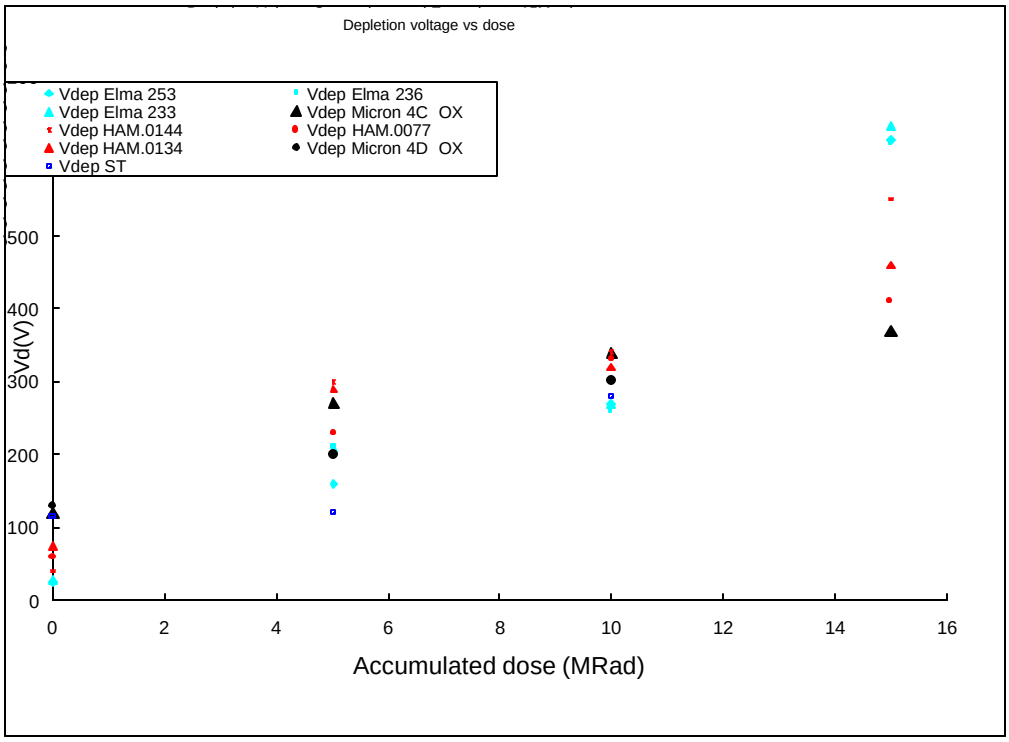

Figure 20. - Depletion voltage as a function of irradation for Run 2B detectors.

Figure 20 shows the measured depletion voltage as a function of dose. The depletion voltage is estimated from the plateau of the detector response to a 1064 nm laser and has ~20% errors. The devices behave roughly as expected, although there is a considerable spread in the depletion voltage at 15 Mrad. The ELMA detectors, which are fabricated using non-oxygenated silicon with a crystal orientation of <111>, have the worst behavior. The spread in depletion voltage is consistent with the variations among silicon types and manufacturers observed by LHC experiments.

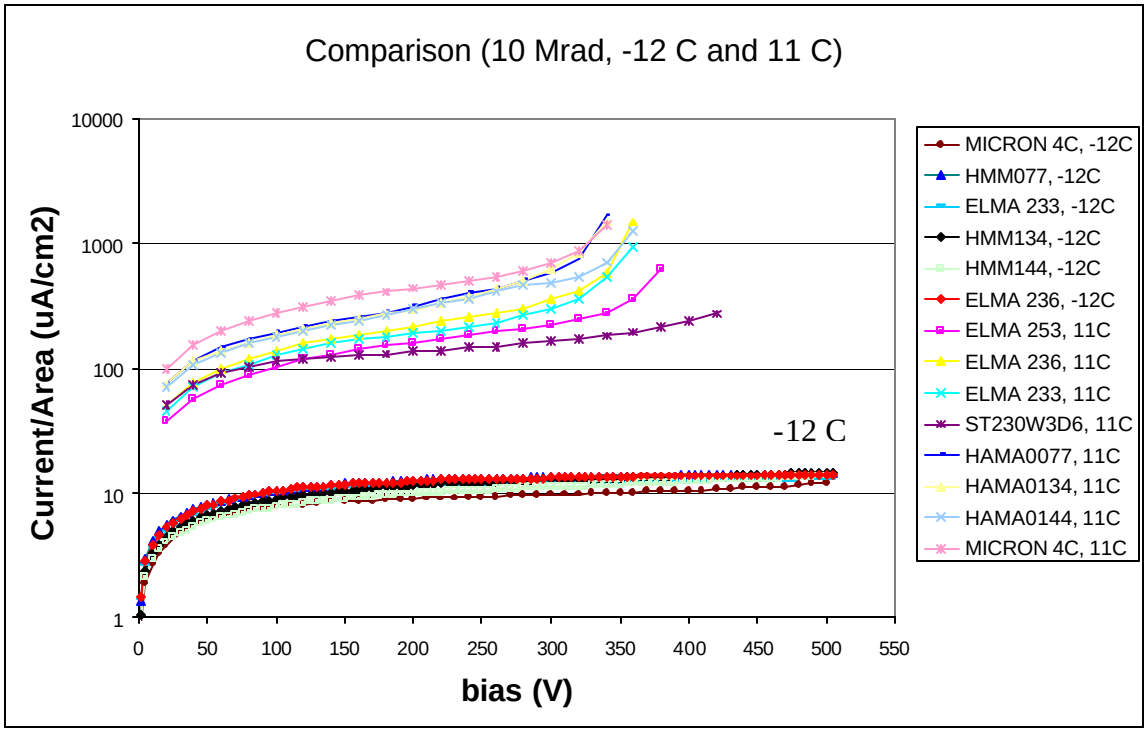

Figure 21. - Leakage currents at +11 and –12 degrees C after 10 Mrad.

Leakage currents for all devices, presented in Figure 21, were found to be consistent with the usual 3 $x10^{-17}$ A/cm^2 damage constant. The breakdown voltage depends on operating temperature as well as annealing time after the intense irradiation. None of the devices showed breakdown before full depletion under laser test conditions (near +10 deg C). Additional operating margin is available at our expected operating temperature of –10 deg C.

The results of these studies give us confidence that we can build a detector which can operate to 15 fb^{-1} and beyond. We plan to irradiate samples of prototype and production detectors to confirm their performance. We also expect to irradiate ladders bonded to SVX4 chips to measure ladder noise performance after irradiation.

4.5 Conclusion

The high integrated luminosity of Run 2B will necessarily result in a particularly harsh radiation environment. Reliable operation of silicon sensors in such conditions is crucial to the experiments success. We were guided in our design and technology choice by our experience in Run 2A detector construction as well as by recent advancements in radiation hard silicon technology motivated primarily by the needs of LHC experiments. In Run 2B DØ plans to use only single-sided single-metal silicon sensors, limiting them to only 3 types. Our estimates, supported by the results of the irradiation tests, show that these sensors will be able to withstand the radiation dose equivalent to 15 fb^{-1} with significant safety margin in layers 1-5. Depletion

voltage in Layer 0 sensors might exceed 700V after 15 fb^{-1}. Oxygenation of these sensors is expected to slow down the depletion voltage growth after the type inversion. Further R&D studies are needed to confirm this approach.

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[7] http://cosmo.fnal.gov/run2b/Documents/riibshort.pdf "Plans for RunIIb".

[8] J. Albert et al. " The relationship between signal-to-noise ratio and b-tag efficiency." CDF Note #3338.

CHAPTER 5 - MECHANICAL DESIGN, STRUCTURES, AND INFRASTRUCTURE

5.1 Overview

The mechanical design of the Run 2B silicon detector is challenging. It must satisfy strict requirements on material mass, on precision of construction and positioning, it must allow for signal readout and cooling of the detectors, and must satisfy overall size constraints imposed by the need to install the detector from the limited space between the calorimeter cryostats. In order to meet the latter requirement, the silicon for Run 2B will be divided about z = 0 into identical north and south barrel assemblies. That division addresses the limited installation space available after the end calorimeters have been opened 39" and allows a net length of silicon associated structures to exceed the 52" that would otherwise be available. Final connections between north and south assemblies will be made via reproducible ball mounts during installation at DØ. Testing and experience with the Run 2A silicon (which is also split at z = 0) demonstrated that a reproducibility of 2 μm is achieved with such ball mounts.

Each assembly comprises six silicon layers and is subdivided into an inner barrel with layers 0-1 and an outer barrel with layers 2-5. Inner and outer barrels will be fabricated individually, mated at SiDet to form either a north or a south barrel assembly, and brought to DØ as a completed, tested assembly. The inner diameter of those assemblies allows installation of a 1" outside diameter beryllium beam pipe through the silicon region after the barrel assemblies are in place at DØ. Figure 22 shows a plan view of the detector while Figure 23 shows an axial view.

In each of the north and south barrel assemblies, a double-walled cylinder, which is integral with the outer barrel, positions and supports a thin (~0.5 mm) carbon fiber reinforced epoxy (CFRE) silicon-positioning membrane near z = 0 and a thicker (~1 mm) CFRE outer silicon-positioning bulkhead at either z = ±500 mm or z = ±600 mm. Studies of coordinate measuring machine (CMM) capabilities and structural deflections will aid in determining which location for the outer bulkhead is better. In either case, a reproducible ball mount connection will be made between the support cylinder of the outer barrel and an additional cylinder extending from the outer positioning bulkhead to the end of fiber tracker barrel 1. The additional cylinder allows better access for precision CMM measurements of silicon positions and better access for work on the ends of silicon sub-assemblies. After all assemblies are in place and all mechanical connections are completed, the equivalent of a single 356 mm outside diameter support cylinder will extend ~1650 mm from one end of fiber tracker barrel 1 to the other.

Silicon sensors of the inner barrel, layers 0 and 1, are mounted on facets of quasi-polygonal cylindrical structures similar to the one used in Run 2A for CDF layer 00. All inner barrel sensors will be placed so that their traces are axial. The inner barrel is supported by the silicon-positioning membrane and by the silicon-positioning bulkhead of the outer barrel. Silicon of the outer barrel, layers 2-5, is contained in 84 staves, which are supported from the silicon-positioning membrane and the outer silicon-positioning bulkhead of the barrel. In order to provide azimuthal overlap between sensors, each silicon layer will be divided into inner and outer sub-layers "a" and "b". Each of the staves of the outer barrel will contain a set of sensors

oriented so that their traces are axial and a set of sensors oriented to provide small angle stereo information. Table 3 gives the radii, lengths, and number of phi segments for the detector.

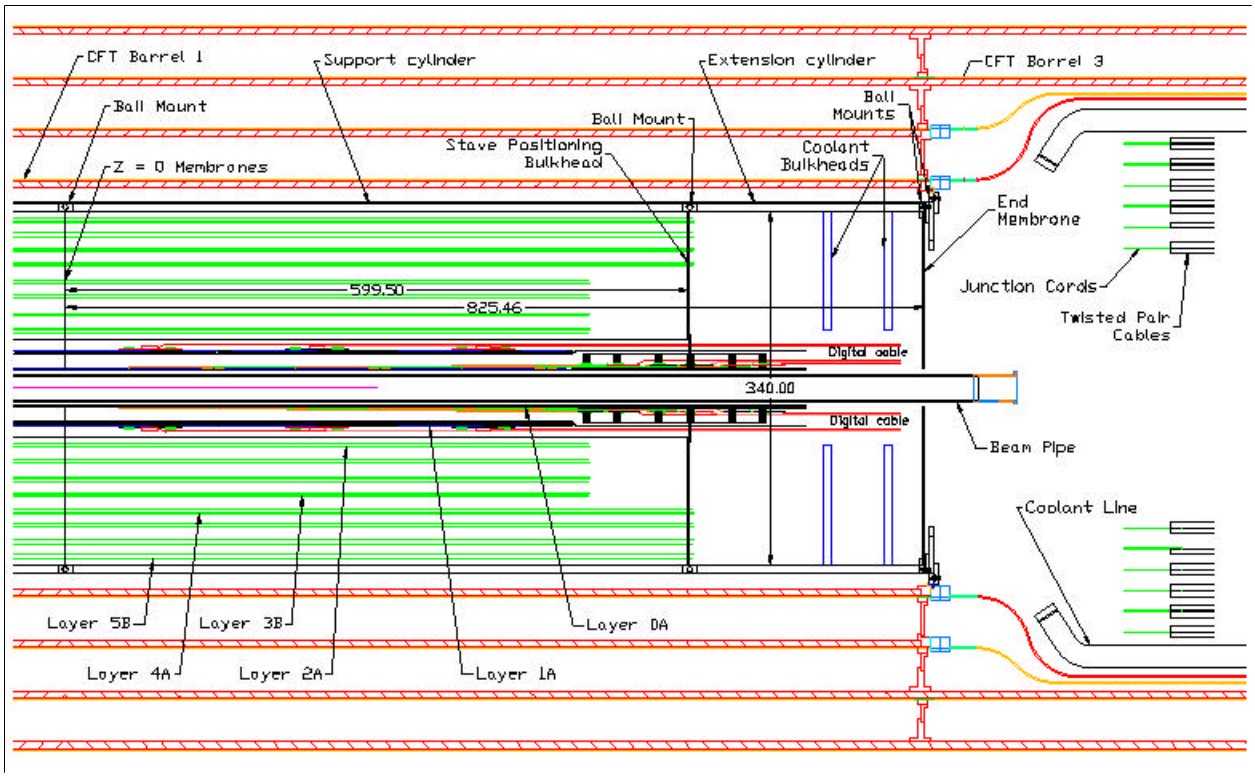


Figure 22 - Plan view of the silicon tracker within the fiber tracker. The silicon tracker is divided into north and south assemblies about z = 0. For each of the assemblies, layers 0-1 and layers 2-5 are fabricated as separate mechanical structures and mated at SiDet. To facilitate CMM measurements, only the portion of the support cylinder from z = 0 to z = 600 mm will be present during layer 2-5 stave installation and mating with layers 0-1. Coolant distribution bulkheads, coolant connecting tubing, and extension cylinders will be added when that work is complete. The lengths of the north and south assemblies match those of the Run 2A central silicon and utilize the Run 2A mounts on the ends of the fiber tracker. North and south assemblies will be joined during installation at DØ to form a full-length structure designed for support only at its ends Lengths of layers have been chosen to provide good acceptance for high p_T physics taking into account the expected length of the luminous region. The silicon of layers 2-5 is shown at the central radii of sensors. CFRE, hybrid, and cooling structures of staves are not shown. In all staves, those structures extend to the z = 600 mm positioning bulkhead. In layers 2-3, only a portion of the stave length is populated with silicon.

Table 3 - Silicon geometric parameters of a barrel assembly (units = mm)

Layer	0a	0b	1a	1b	2a	2b	3a	3b	4a	4b	5a	5b
R axial	18.6	24.8	34.8	39.0	53.2	68.9	89.3	103.4	116.9	130.6	150.1	163.6
R stereo	---	---	---	---	56.3	72.0	86.2	100.3	120.0	133.7	147.0	160.5
Length(z)	475	475	475	475	501	501	501	501	601	601	601	601
# Phi	6	6	6	6	6	6	9	9	12	12	15	15

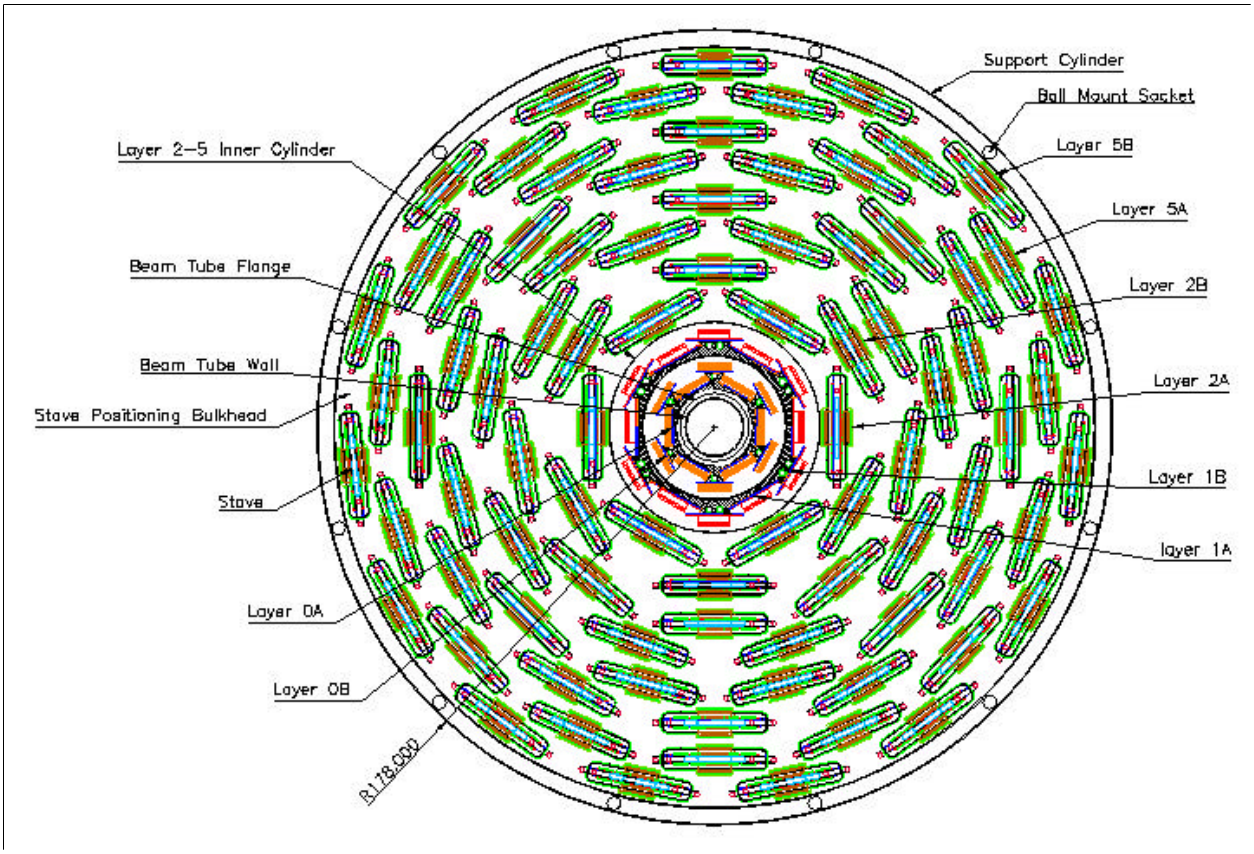


Figure 23 - End view of the layer 0-1 module, layer 2-5 staves and the outer silicon-positioning bulkhead. Silicon radii and sensor widths have been chosen to provide >99% r-phi geometric acceptance for tracks of p_T > 1.5 GeV/c originating within 2 mm of the nominal beamline. The design of the layer 0-1 and layer 2-5 assemblies allows removal of layers 0-1 at DØ and replacement with good precision. The inner diameter of layer 0 has been chosen to permit beam pipe installation after all silicon is in place at DØ.

5.2 Overall Support Structure

The main structural components must provide accurate, stable positioning of both the inner and outer detector elements. The main components are a double-walled carbon fiber cylinder that resides outside the outermost silicon layer and a set of bulkheads that provide the precision mounting points for the outer layer staves and the inner layer sub-assemblies. The details of these components and the alignment constraints are provided in the following sub-sections.

5.2.1 Outer support cylinders, stave positioning bulkheads, and z = 0 membranes

The design of the 356 mm outside diameter support cylinders is based upon that of the 306 mm outside diameter cylinders of Run 2A. Each cylinder will have inner and outer CFRE walls ~0.56 mm thick separated by CFRE "ribs" ~0.40 mm thick. Seven or more layers of flame retardant free, high modulus (>90 MSI), unidirectional fiber prepreg will be used for the shells and six or more layers for the ribs. The number of layers will depend upon the thickness of the high modulus material which is available. Individual CFRE pieces are cured at elevated temperature and then bonded to one another at room temperature with epoxy. Based upon the performance of the Run 2A cylinders, beam deflection should be less than 40 μm over a length of 1650 mm. Compensation for that deflection can be made by offsetting either the z = 0 positioning membranes or the outer positioning bulkheads when they are glued to the cylinder. The ribs, end rings, membranes, and bulkheads stiffen the completed structure against out-of-round distortions. Based upon performance of Run 2A cylinders before openings were cut for silicon installation, out-of-round distortions should be minimal. However, prototypes will need to be fabricated and measured to verify beam and out-of-round deflections. Mandrels of appropriate diameter and cylindricity, appropriate fixturing for gluing operations, an oven, and a sufficiently large CMM will be needed. We anticipate that the majority of the cylinder fabrication would be done in Lab 3, but CMM measurements might be done at SiDet.

The CFRE stave-positioning bulkhead will be made of multiple layers of flame-retardant-free, high modulus (>90 MSI), unidirectional fiber prepreg with an elevated temperature cure. To match the ~0.75 mm thickness of stave locating bearings, the bulkheads are expected to be 1 mm thick. Openings in the bulkheads are intended to match stave profiles, including cables, and to provide 0.5 mm clearance about the full stave periphery. Staves will be installed through the openings and located by pins which engage locating bearings glued into the bulkhead. We plan to cut oversized openings for the bearings and to locate the bearings using high-precision fixturing as they are glued into place. The intent is to place the stave locating bearings and the stave pins which engage them well enough to allow interchangeability among staves. Arrangements have been made with Lab 8 to begin cutting stave and bearing openings in a prototype positioning bulkhead to provide a general test of this stave positioning concept (Figure 24). The CFRE material that was provided to Lab 8 has a high modulus but contains flame retardant, so the resultant piece will be used for test purposes only.

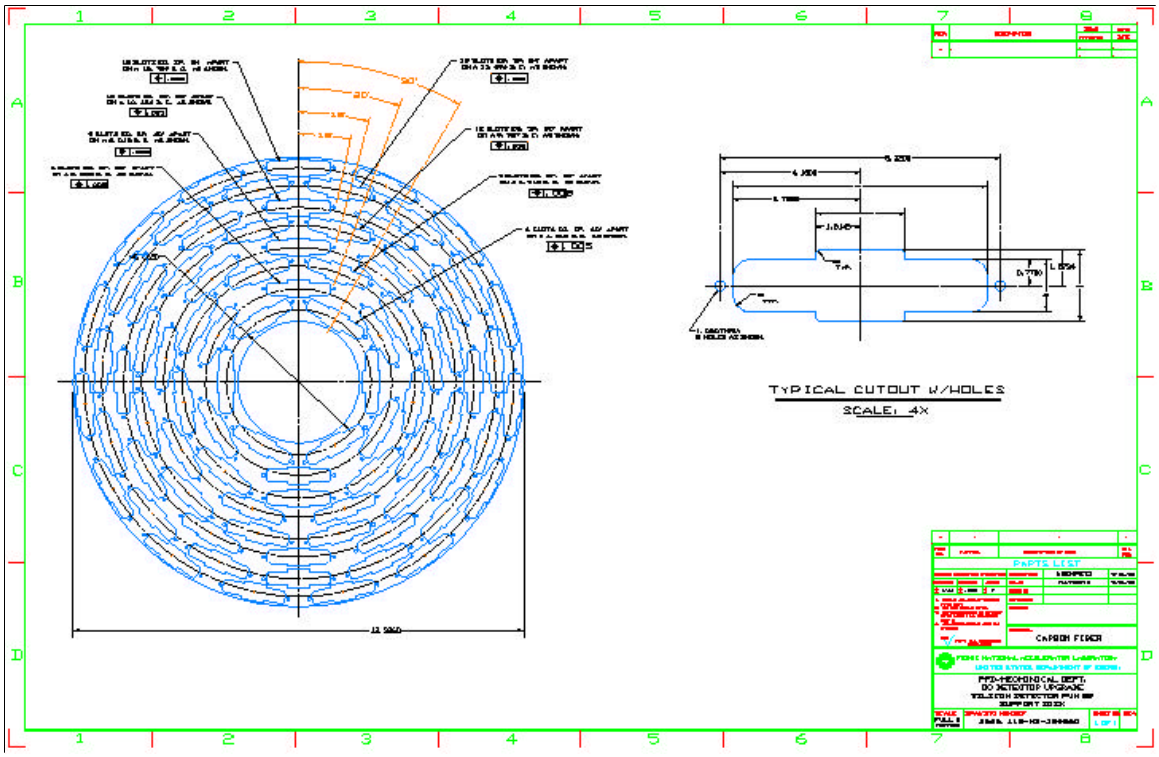


Figure 24 - Cut profile supplied to Lab 8 for a prototype positioning bulkhead. The profile of a stave opening is shown on the right; the locations of openings are shown on the left.

The CFRE z = 0 membrane will be made of multiple layers of flame retardant free, high modulus (>90 MSI), unidirectional fiber prepreg with an elevated temperature cure. In principle, the membrane could be a full disk with an opening for the beam pipe, since staves do not pass through it. In practice, openings will be cut in the membrane to reduce material. A design for the openings remains to be developed. Bearings will be glued into oversized openings in the membrane to engage stave-positioning pins. Local reinforcement will be provided at each bearing location. A precision fixture will be used to position bearings as they are glued into place.

CFRE end rings for each cylinder include sockets of the ball mounts and features to allow one cylinder to be securely coupled to the next. Based upon Run 2A experience, twelve ball mounts, evenly space in azimuth, should be sufficient per end ring. Screws or studs through the balls will be used to couple cylinders. Openings through the outer walls of cylinders, with suitable reinforcement, will provide access to install and tighten fasteners. The end rings will be made of multiple layers of flame retardant free, high modulus (>90 MSI), unidirectional fiber prepreg with an elevated temperature cure. Precision jig plates will be used to position the ball mount openings.

A CMM will be needed as pieces of cylinder assemblies are glued to one another in order to establish clockings and offsets. Whenever practical, end rings will be mated during the gluing process. A full procedure for establishing end ring clockings and offsets remains to be developed. In general, we plan to employ ruby or sapphire balls as reference features for CMM

touch probe measurements. Positions of stave locating features can be measured in a coordinate system established by these reference features.

5.2.2 Alignment precision and survey accuracy

All alignment constants, both at the trigger level and offline, assume that the silicon sensors are perfect planes. Six constants are used, three offsets used to define the position of the center of the sensor and three Euler angles used to define the rotations of the sensor about that center. Survey data taken during assembly, or obtained from offline alignment with tracks, can be used to determine the alignment constants for the tracker. No real-time alignment constants are available so it is critical for the trigger that the detector be stable over time scales of weeks to months.

It is important to make a clear distinction between the precision required for the placement of the sensors and the required survey accuracy. The physical alignment precision for the sensors is determined primarily by the requirements of the impact parameter trigger, which is used to identify events with tracks originating from the decay of heavy quarks outside the beam spot. Having satisfied these constraints, other considerations, such as having tractable offline alignment constants, are also satisfied. The survey accuracy, whether done using optical or mechanical survey on the bench, or using tracks *in situ*, should have accuracy on the scale of the intrinsic device resolution (≈8μ transverse to the sensor strips).

No stereo information is available at the trigger level so the trigger is most sensitive to rotations about the two axes transverse to the beam line (pitch and yaw) that result in Z-dependent ϕ errors. Deviations from planarity are also important, both at the trigger level and for the offline analyses since these are not corrected for. The figure of merit for location of sensors is that, relative to the beam spot size, the errors introduced have a small effect on the impact parameter resolution. For a rotation about an axis perpendicular to the plane of the sensors (yaw), the desired alignment tolerance is <10μ over the length of a readout segment. The pitch angle affects strips at the edges of the sensors, but not at the center. For a radial deviation dR at an angle ϕ from the center of the sensor, the transverse measurement error dX is given by $dX=dR\tan\phi$. Local radial displacements due to a lack of sensor flatness contribute in the same way as an overall pitch of the sensor. Again, the desired tolerance is dX<10μ within a readout segment.

5.3 Layer 0-1 Silicon Mechanical Support Structure

5.3.1 Introduction

The Layer 0 and 1 silicon support structures described in this TDR are carbon fiber structures with each layer consisting of an inner and outer carbon fiber shell, with graphite foam and/or pyrolytic graphic that transfers heat to the cooling tubes inserted between the inner and outer layers. Our conceptual design borrows heavily from the CDF inner silicon support structure that is also made from carbon fiber composite. We are currently exploring two fabrication processes; the RTM (Resin Transfer Molding) process or the use of unidirectional pre-preg materials. We have chosen "PEEK" (Poly-Ether-Ether-Ketone) as the material for the cooling tube and we also

have developed a full solid model of the design and coupled that to the FEA analysis using ANSYS in order to establish structural properties of the support structures. A preliminary analysis of a fully loaded (silicon, cables, cooling tubes, etc.) has been performed and the maximum sag expected for the inner layer, supported as described herein, is 5.8 microns. The remaining work requires the development of a full design, sufficient prototype work to certify the fabrication techniques, a final detailed FEA analysis that includes thermal conductivity analysis, and the production of a final solid model, from which assembly and production drawings can be produced.

Cost estimates are based on this design concept and the contingency analysis is performed by first assigning risk factors from which weighting factors are calculated, then multiplying the weighting factors and summing to determine a composite contingency percentage. This is done for each element at its lowest level.

5.3.2 Design

The silicon sensors and associated electronics in layer 0 and layer 1 require a very lightweight and rigid support structure, constructed to very demanding mechanical tolerances. Provision must also be made for cooling of the sensors and the hybrid electronics. Carbon fiber/epoxy composite provides the most effective combination of low density and rigidity along with manufacturing flexibility.

L0 Structure:

The L0 support (Figure 25) consists of a backbone tube and an outer, castellated ring on which the sensors are mounted.

The space between these is filled with carbon foam to provide a shear connection and to act as a thermally conductive layer to transfer heat from the sensors to cooling tubes embedded in the foam (Figure 26). This structure extends from Z=0 to Z=485 mm.

The hybrids are mounted separately from the sensors on structures that extend out to Z=710 mm (Figure 27). This structure has six support rings (one per hybrid) to both hold the hybrids and to provide a heat flow path for cooling. Six carbon/epoxy stiffening ribs connect these rings. To provide further bending stiffness, the inner carbon/epoxy tube has its wall thickness doubled in the region of the hybrids.

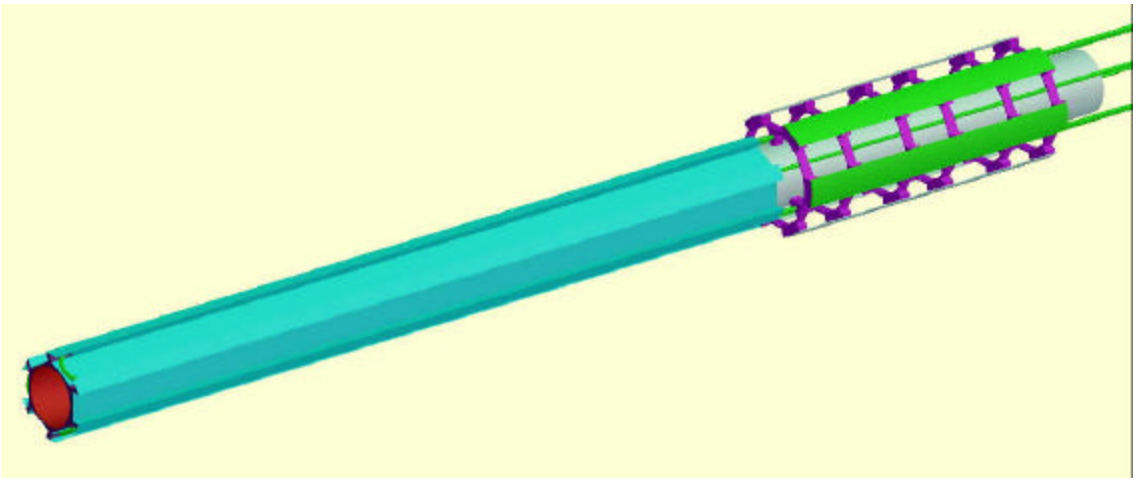


Figure 25 - L0 mechanical structure

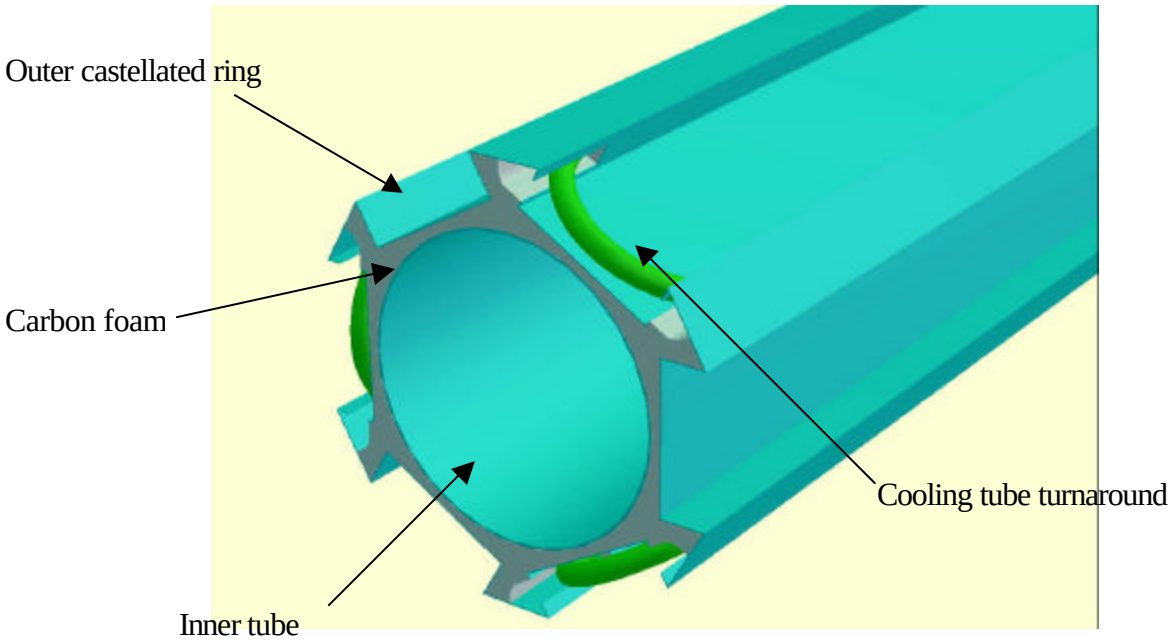


Figure 26 - Detail of silicon support and cooling tubes.

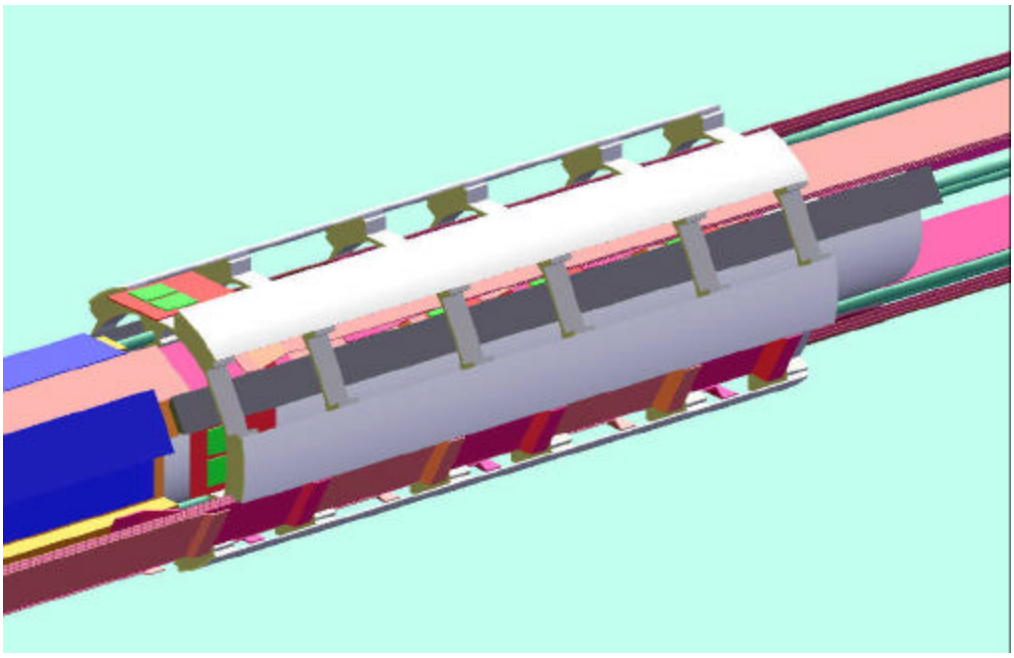


Figure 27 - L0 hybrid support structure

The silicon sensors are mounted on the castellated tube using adhesive. An insulating layer of Kapton separates the silicon from the conductive carbon/epoxy.

Note that there are two layers of these sensors at different radii (layers 0a and 0b). Analog cables connect each sensor chip to its specific hybrid chip. A PEEK cooling tube is embedded in the carbon foam below each of the outer silicon chips. All of these features are shown in Figure 28. A water/glycol mixture circulates through these tubes to maintain the desired chip temperature. The flow is turned around at Z=0 as shown in Figure 26.

The hybrid circuits are individually attached to their support rings and digital cables lead from each chip to connections external to the support structure. (Figure 29).

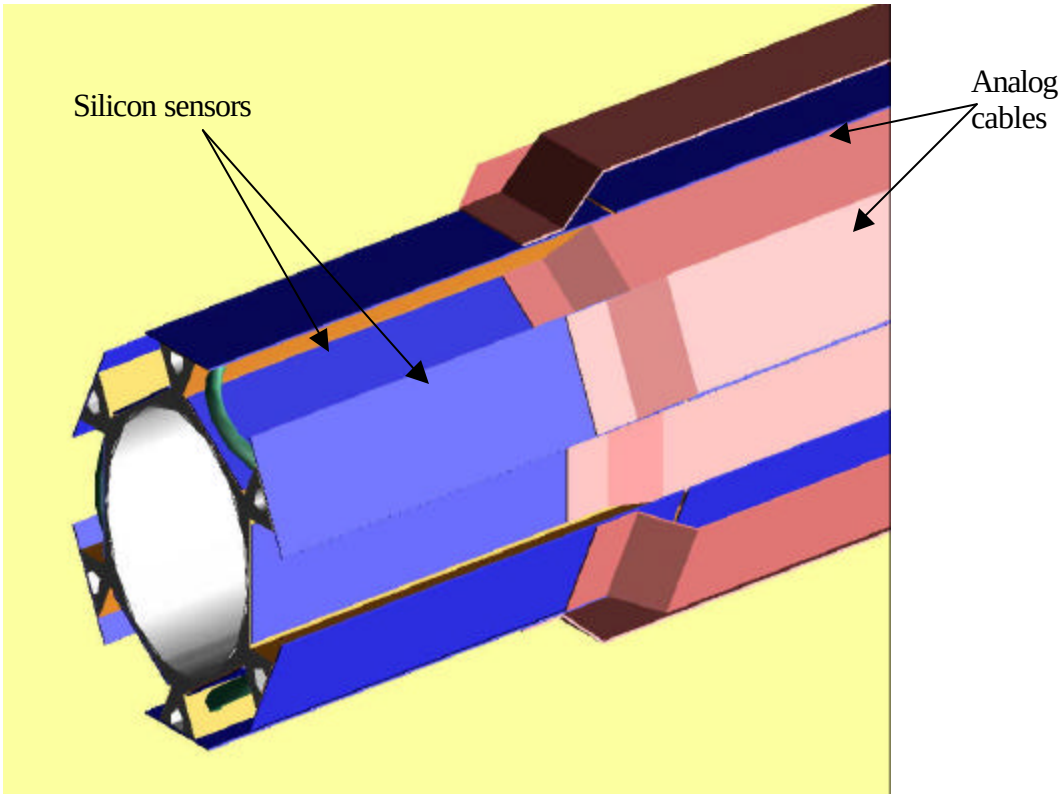


Figure 28 - Silicon sensors and analog cables.

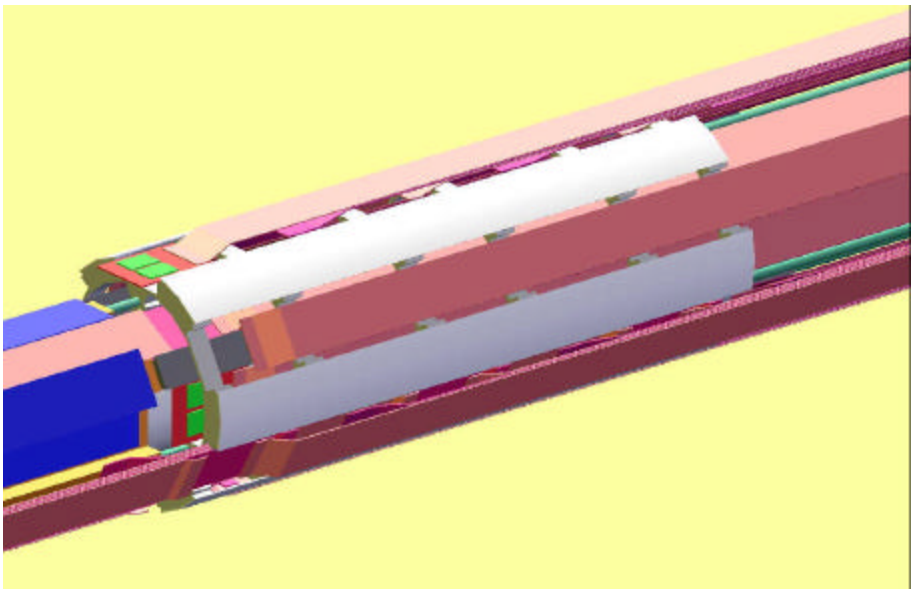


Figure 29 - Hybrid chips and digital cables

L1 Structure

This is very similar to L0. The major difference is that the hybrid circuits are mounted directly on the silicon sensor chips and only digital cables connect these to the outside world (Figure 30).

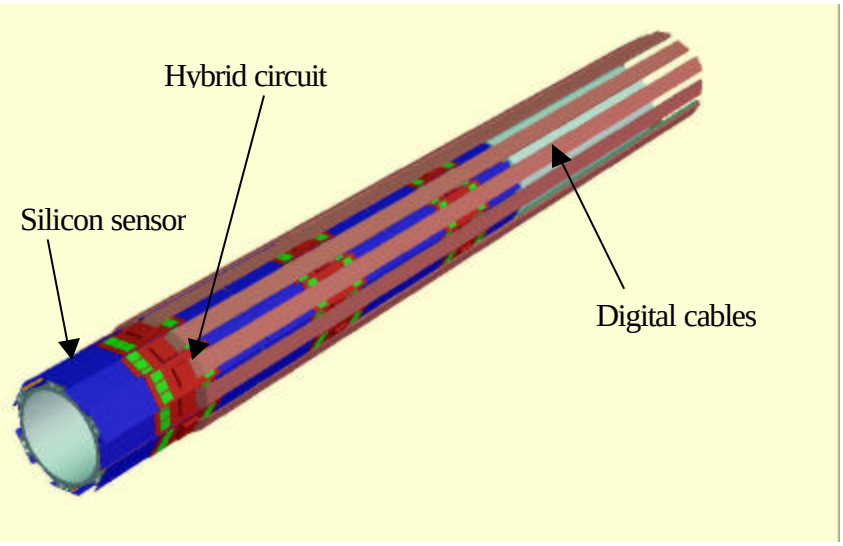


Figure 30 - L1 assembly complete with silicon sensors, hybrids and digital cables.

The sensors are mounted on a structure consisting of two carbon/epoxy rings separated by carbon foam. Cooling tubes are embedded in the foam as in L0. This is all shown in Figure 31.

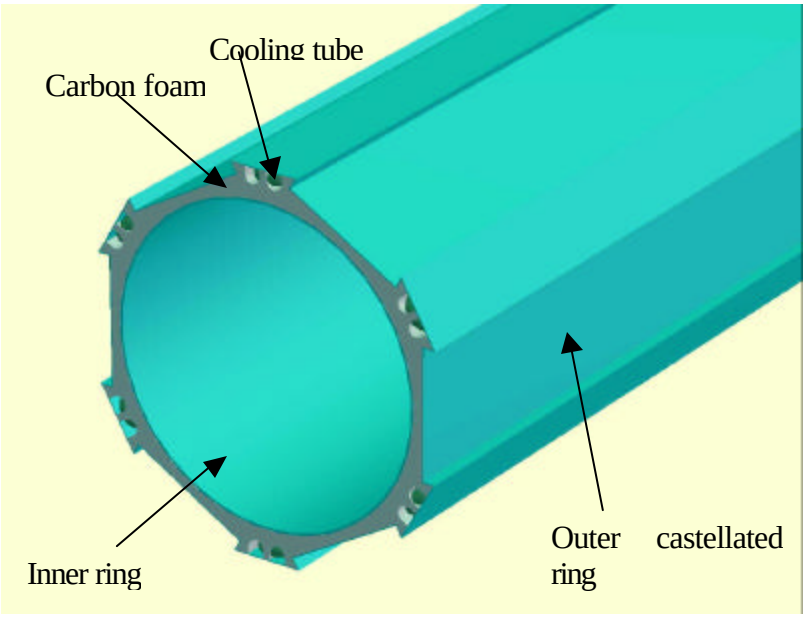


Figure 31 - L1 carbon fiber/epoxy structure

L0/L1 Assembly

The L0 and L1 mechanical structures have to be assembled into a single structure after the silicon, hybrids and cables have been attached (Figure 32).

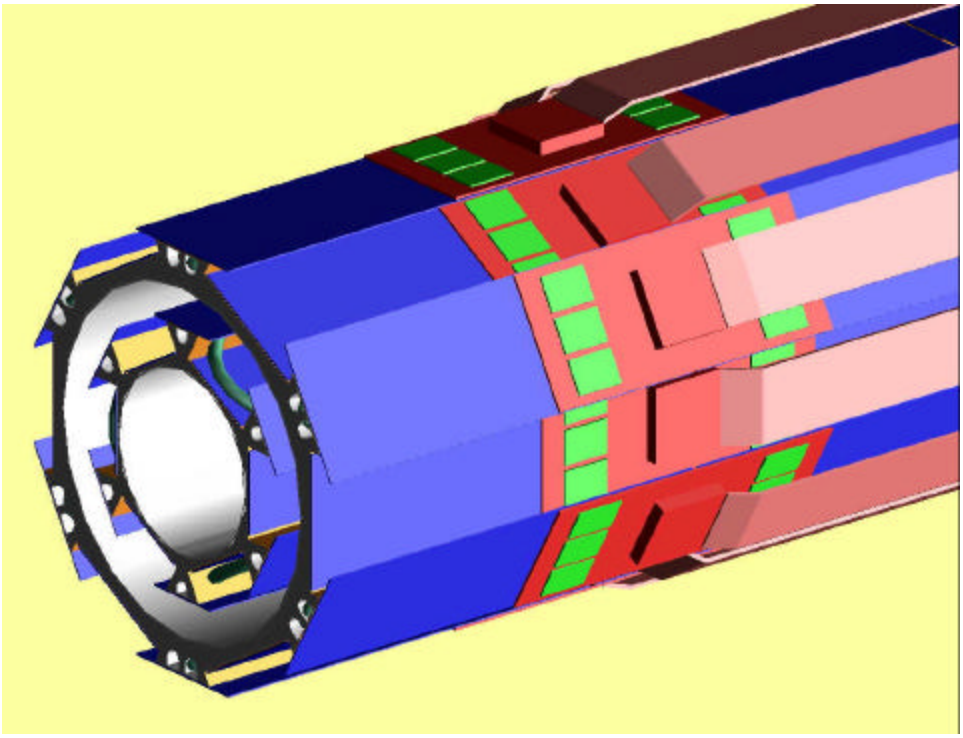


Figure 32 - L0/1 assembly

At Z=0 this is accomplished by a simple membrane made from carbon/epoxy. This membrane has precision pin fittings that locate L0 and L1 to the membrane. Another set of such pins locates the membrane to the L2/L5 support structure. At Z=630 mm, the L0 structure is connected to the inner surface of the L1 structure via the hybrid support ring at that location. This connection will also use precision pins so that L0 is located in a precise position within L1. The outer surface of the L1 structure is connected to the L2/L5 structure in a similar way. To avoid any backlash problems, all of these connections will be spring loaded against precision stops. (At the time of writing, detailed design concepts for all of these connections are not available).

Radiation Lengths

The total radiation length in the tracking volume is calculated to be 1.63% and 2.42% for L0 and L1, respectively. In the end regions where the combined L0 hybrids are located the radiation length is about 4.43%. In these calculations discrete objects such as cables and hybrid circuits are uniformly distributed over the sensors that they overlap.

The total material/radiation length presented by Layers 0 and 1 is summarized in the Radiation Length Calculation tables found in Appendix 5.3.A.

5.3.3 FEA analysis of the L0/L1 mechanical structures

The high precision required in the silicon support structures implies that these very light structures must also be very stiff. The design process must be accompanied by detailed structural analysis using FEA methods. At present, this has been done for the proposed design of the L0 structure. Given that the results appear very promising, these studies will be extended to the L1 structure.

The existing Unigraphics CAD solid model was used as the basis of the FEA model. Solid models of the structural parts of the L0 CAD model were transferred to Ansys v5.7 for FEA analysis. The models of each part were first broken up into sets of volumes convenient for generating the FEA mesh in Ansys. The FEA model included the carbon/epoxy inner tube, outer castellated ring and carbon foam at the silicon sensor end. The hybrid carbon/epoxy inner tube and stiffeners were added along with the six beryllium support rings.

The model was transferred over as a 60° slice of the support. This was then meshed and then copied to form a 180° symmetric half model. This is shown in Figure 33.

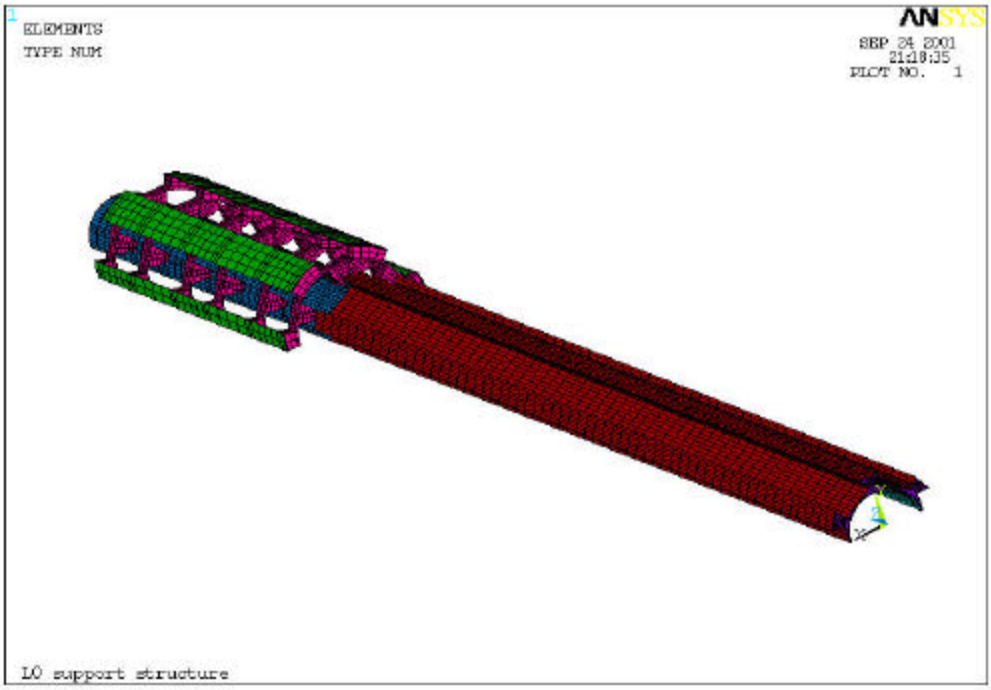


Figure 33 - FEA model of the L0 support structure

The silicon end is shown in detail in Figure 34. The two carbon rings and the carbon foam structure are modeled along with the slots in the foam for the cooling tubes. The hybrid end of the model is shown in detail in Figure 35.

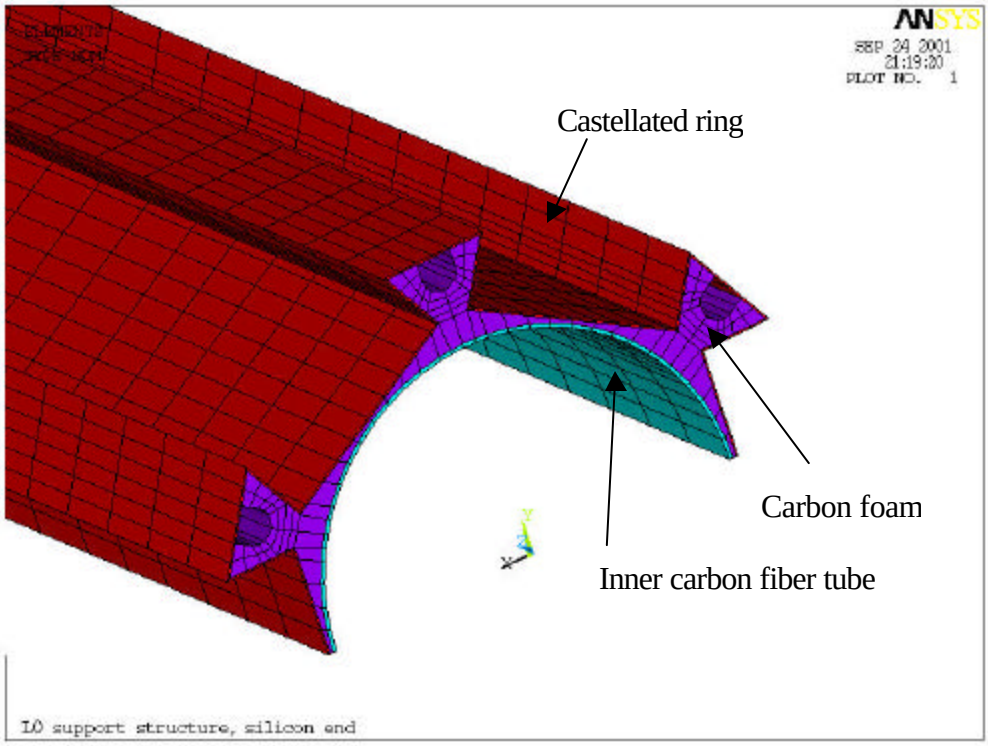


Figure 34 - details of FEA model at silicon support

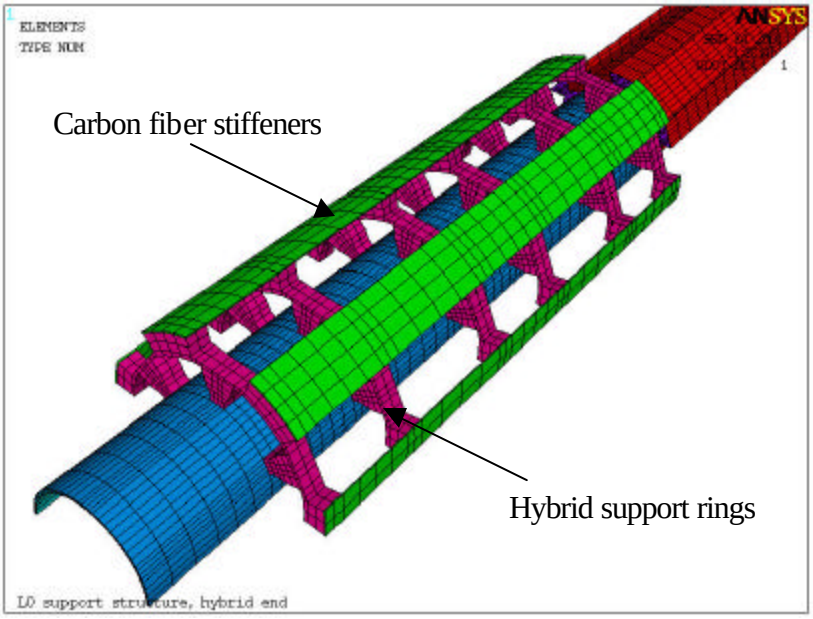


Figure 35 - details of FEA model at hybrid support end

The carbon/epoxy was assigned linear, orthotropic elastic properties and these are detailed in Table 4. The carbon foam was assigned a linear isotropic elastic modulus of 2.0 GPa and the beryllium rings had the standard modulus (303 GPa) for that metal. The carbon /epoxy had a density of 1540 kg/m^3, the foam was 200 kg/m^3 and beryllium was 1850 kg/m^3.

Table 4 - Orthotropic properties of carbon fiber/epoxy composite material. Note: the Z-axis is along the length of the structure.

E_x	26	GPa
E_y	26	GPa
E_z	127	GPa
G_{xy}	22	GPa
G_{yz}	22	GPa
G_{xz}	22	GPa
ν_{xy}	0.69	
ν_{yz}	0.69	
ν_{xz}	0.69	

The model was simply supported at location at Z=0 and Z=630 mm. Symmetry boundary conditions were imposed along the open edges of the model. It was loaded by gravity and the weights of the cables, silicon sensors, hybrid circuits, cooling tubes and coolant were included as point and/or distributed loads as appropriate. The total weight of one end of L0 was predicted by Ansys to be 180 g.

The deflection solution is shown in Figure 36 and a plot of deflection versus distance from Z=0 is shown in Figure 37. The maximum sagitta was 5.8 microns. The limitations of this FEA model need to be considered:

1. FEA analysis of this complexity is usually accurate to within 10 to 15%.

2. The properties of the carbon/epoxy need to be verified by experiment. The values used were obtained by prediction using standard classical lamination theory. They are reasonably conservative.

3. The hybrid support rings will most likely not be made from beryllium. However, they do provide an essential heat flow path for cooling the hybrids. Carbon foam is a possible alternative material. Note that one of these rings will be used to support L0 within L1 and its mechanical properties are, thus, more critical.

4. No account has yet been taken of external loads from cables and cooling lines.

5. Thermally induced deflections have not yet been studied.

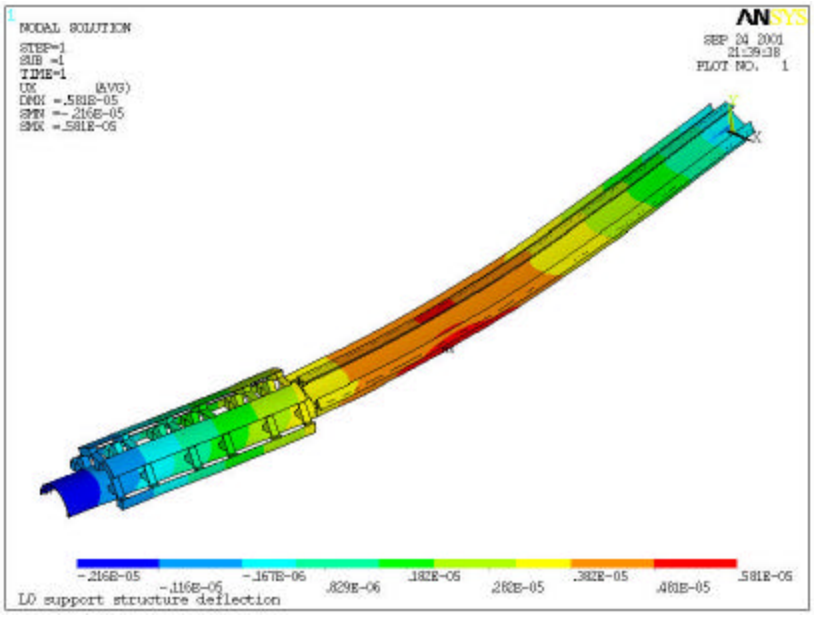


Figure 36 - Deflection solution

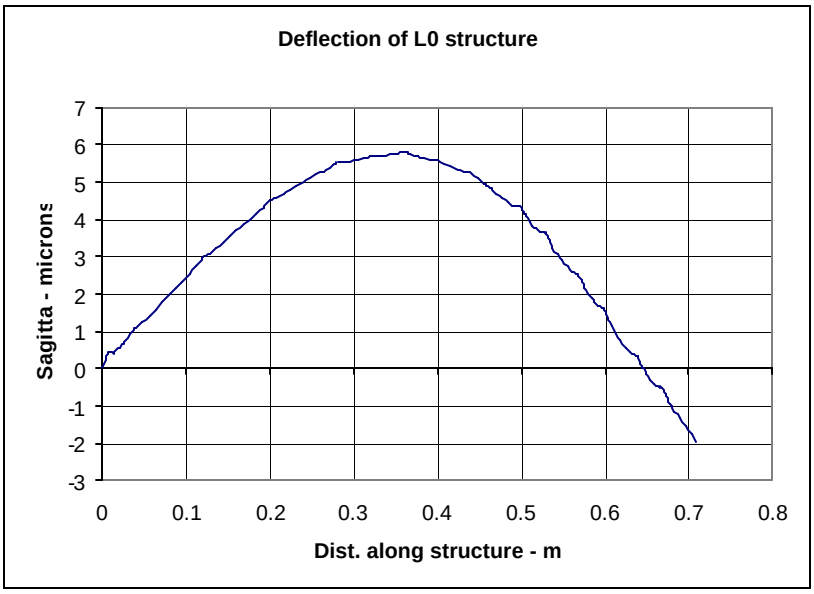


Figure 37 - Deflection vs. distance along structure from Z=0

The above issues can be studied readily using this FEA model. Material properties can be changed easily and heat conduction studies carried out along with determination of the resulting thermal deflections.

5.3.4 Fabrication techniques

A cross-section of the preliminary design for the L0 support structure is shown in Figure 38. The cross-section is an assembly involving an inner and outer carbon/epoxy composite shell, embedded cooling tubes, graphite foam core material, annealed pyrolytic graphite films, and kapton films. The outer shell has a castellated profile, which allows mounting silicon detectors at two radial locations.

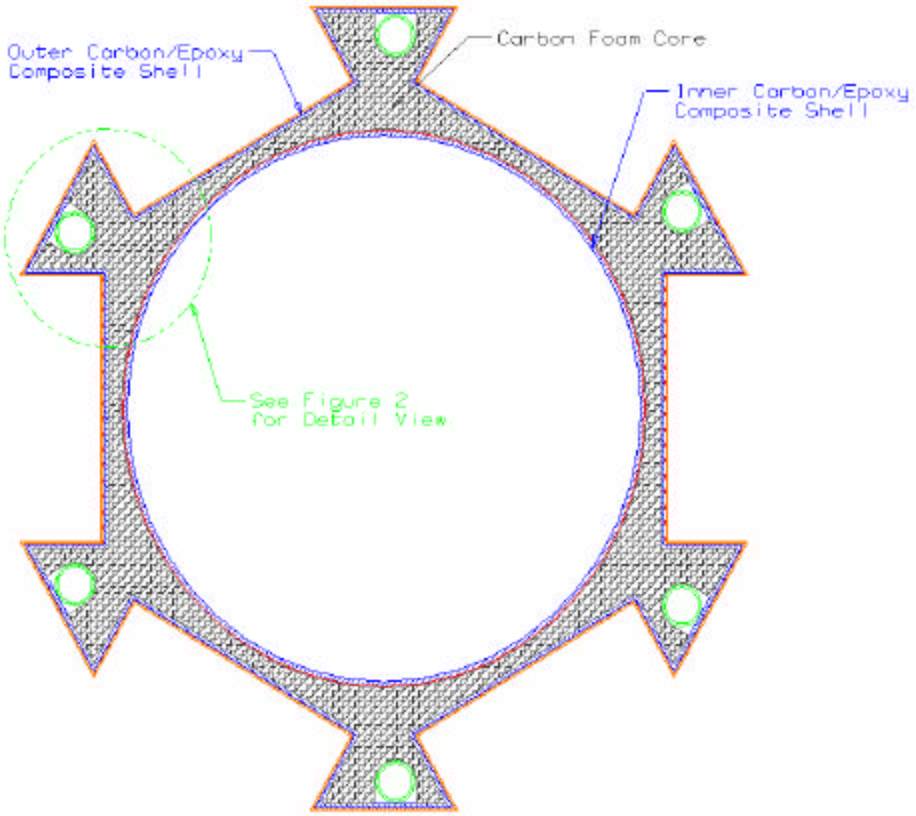


Figure 38 - Cross-section of the L0 support structure (preliminary design)

A detail of a typical castellated region is shown in Figure 39. Graphite foam will be used as a core material in this region. PEEK cooling tubes will be embedded within the graphite foam, and annealed pyrolytic graphite films will be bonded to the surface of the carbon/epoxy wall laminates. The use of a graphite foam core and pyrolytic graphite films will provide high thermal conduction between the silicon detectors and the embedded cooling tubes. A flat kapton film will be bonded to all surfaces that support the silicon detectors. The kapton film will serve as an electrical insulator between the silicon detectors and the underlying substrate.

Two different methods of producing the carbon/epoxy shells are under investigation: use of unidirectional pre-preg tape, or the use of resin-transfer molding (RTM) in conjunction with a

braided tubular preform. Both techniques have advantages and disadvantages, as explained in the following paragraphs.

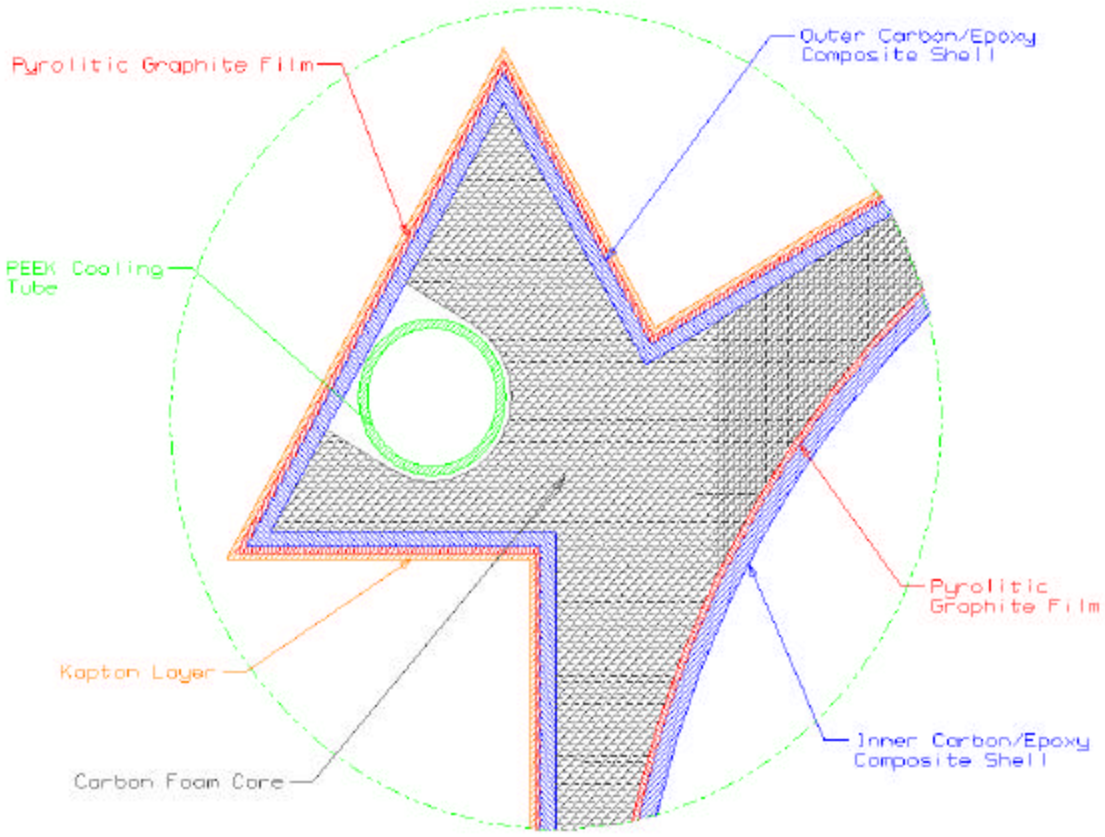


Figure 39 - Detail view of a castellated region of the cross-section shown in Figure 38

The tooling and fabrication procedures used to produce the carbon/epoxy shells using unidirectional pre-preg tape are illustrated in Figure 40. Hard tooling will be used to form both surfaces of the shells, since high-quality surfaces are required. Since pyrolytic graphite film bonds readily to epoxy, it should be possible to place the graphite film within the mold and bond it to the outer surface of the shell during cure of carbon/epoxy pre-preg.

One difficulty associated with the use of unidirectional pre-preg tape has to do with the achievable shell wall thickness. The composite system used will be based primarily on the ultra-high modulus pitch fiber K13D2U. A 0.003 in thick unidirectional pre-preg system based on the K13D2U fiber is available. The laminate stacking sequence for both the inner and outer shells must be symmetric to minimize thermal distortions. A 3-ply [0°/90°/0°] laminate is symmetric and would have a thickness of 0.009 in, but would posses very low shear stiffness. The FEA analyses conducted to date have been based on properties corresponding to symmetric 6 ply laminates with stacking sequences of the type [0°/θ°/-θ°/-θ°/ θ°/0°], where θ = the bias fiber

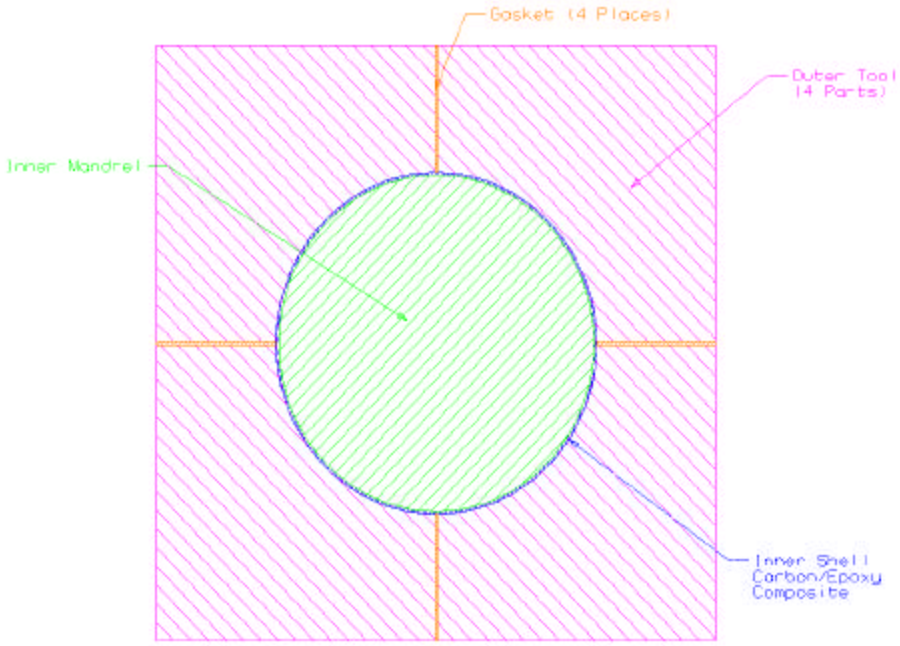


Figure 40 - Tooling used to produce inner carbon/epoxy shell

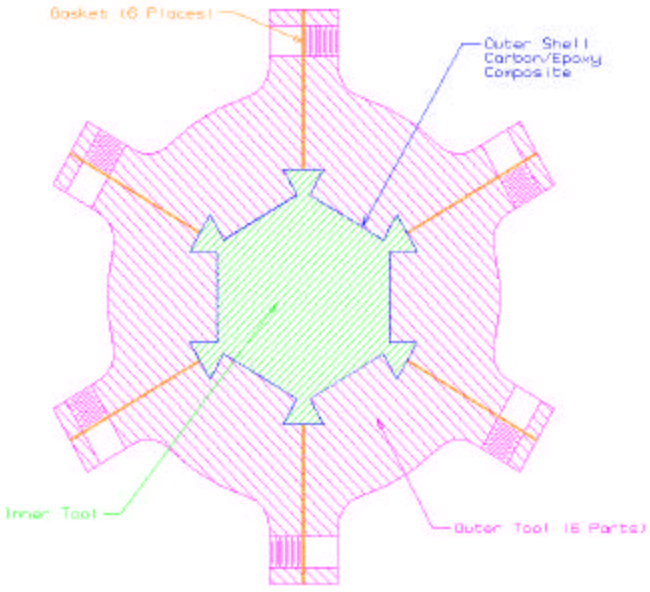


Figure 41 - Tooling used to produce outer carbon/epoxy shell

orientation measured with respect to the long axis of the support structure. Depending on angle θ, this stacking sequence results in acceptably high axial, circumferential, and shear stiffnesses. However, a 6-ply laminate produced using 0.003 inch-thick pre-preg will result in a shell wall thickness of about 0.018 in. If both the inner and outer shells are produced using a 6-ply stacking sequence, then the total wall thickness of the completed structure will be about 0.036 in, which is approximately 50% thicker than the target wall thickness. Appropriate stacking sequences for use with the inner and outer shells are still under investigation. It may be possible to use a 3-ply [0°/90°/0°] laminate for the inner shell and a 6-ply type [0°/θ°/-θ°/-θ°/ θ°/0°] laminate for the outer shell, resulting in a total wall thickness of about 0.0027 in.

A second difficulty has to do with the allowable bias angle θ. Ideally, maximum design flexibility would be achieved if θ could be selected to be any angle within the range 0° to 90°. However the K13D2U fiber exhibits a low strain to failure; the minimum radius of curvature that this fiber can withstand without fracture is estimated to be about 1.5 mm. This minimum radius of curvature ultimately limits the bias orientation that can be used in the outer castellated shell, since the bias fibers must conform to the small radii of curvatures shown along the periphery of the outer shell in Figure 38. Preliminary estimates indicate that for a 0.5 mm radius of curvature (measured in a plane transverse to the long axis of the structure), the maximum bias angle that can be used with the K13D2U fiber is about 20°. Prototype outer shells will be produced using this bias angle and inspected using a SEM to evaluate fiber condition. If excessive failure of the K13D2U fibers is found during this inspection, then either the bias angle will be reduced, or an alternate 0.003 in thick pre-preg system based on a fiber that exhibits a higher strain to failure (T300, for example) will be used in the bias plies.

The kapton film will be bonded to the silicon support surfaces after the outer shell has been cured. A kapton film that can be adhesively bonded is commercially available from Dupont (this product is known as "Type HN" kapton film). The bonding process will be performed using simple flat molds.

An alternate fabrication technique is to produce the carbon/epoxy shells using RTM in conjunction with a triaxial braided tubular preform. An apparent disadvantage of this approach is that, due to fiber waviness and (typically) lower fiber volume content, braided composites usually possess a lower specific stiffness than comparable composite laminates produced using unidirectional plies. However, since a triaxial braided ply is symmetric and yet possesses three fiber orientations, it may be possible to achieve sufficient stiffness through the use of only one or two braided plies, rather than 6 plies as in the unidirectional pre-preg option. Hence, it may be possible to produce a braided structure with sufficient stiffness, and yet with a thinner wall than is possible if unidirectional pre-preg is used. The minimum wall thickness that can be achieved using a tubular braided preform based on the K13D2U fiber is currently under investigation.

The limitations on bias angle (discussed in a preceding paragraph in connection with the use of pre-preg tape) will also be encountered in a braided composite structure. It may be that the K13D2U fiber is too brittle to be used as the bias tows in the castellated outer shell, due to the small radii of curvatures. If this proves to be the case then a braided preform with bias tows based on a fiber that exhibits a high strain to failure (T300, for example) and axial K13D2U tows will be investigated.

The tooling necessary to produce a structure using RTM and a braided preform would be very similar to that shown in Figure 40. The major differences would be that resin injection ports and vacuum evacuation ports are required in the tooling end pieces for the RTM approach. Also, it will not be possible to incorporate the pyrolytic graphite film with the RTM approach. If the graphite-shells are produced using a braided composite then both the pyrolytic graphite and kapton films (where appropriate) will be adhesively bonded after the curing of the shell.

Final assembly of the support structure will be completed once the inner and outer shells are produced. The assembly process currently envisioned is summarized in Figure 42 - Figure 46. The inner graphite shell will be adhesively bonded within a cylindrical cavity in a rectangular block of graphite foam (Figure 42, Figure 43). A high-speed grinding wheel will be used to shape the graphite foam to the desired shape (Figure 44). A cavity for the PEEK cooling tube will also be provided. The cooling tube will then be dropped into this cavity and adhesively bonded to the graphite foam core (Figure 45). Next, a liquid adhesive will be spread over the outer surface of the assembled inner shell/foam core/cooling pipe. The outer carbon/epoxy shell will then be slid over this assembly, while the adhesive is still liquid. The entire structure will then be heated to cure the adhesive, forming an adhesive bond between the inner and outer shells and between the outer shell and graphite foam core. Finally, the kapton film will be bonded to the silicon detector support surfaces of the outer shell, completing assembly of the support structure (Figure 46).

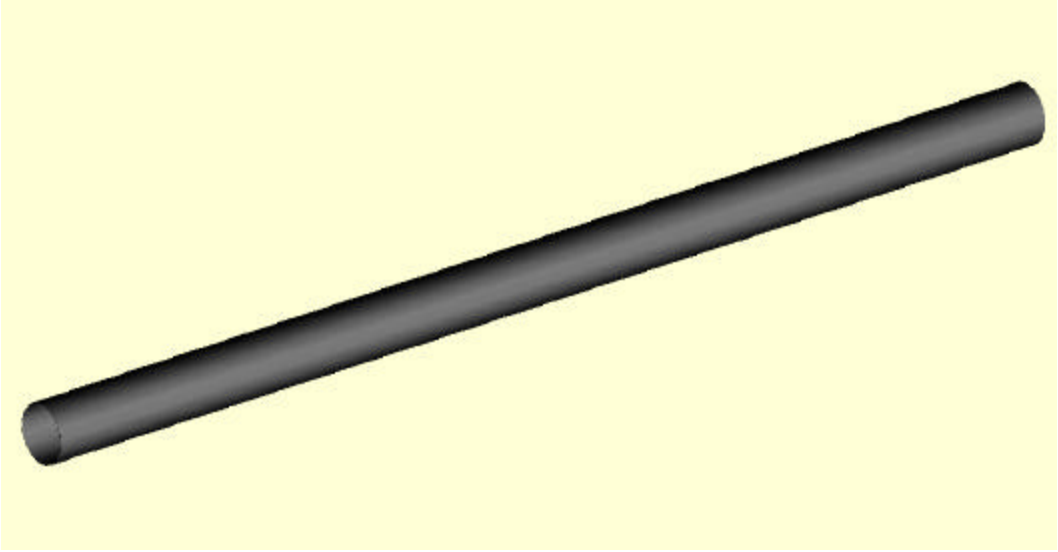


Figure 42 - Finished carbon/epoxy inner shell

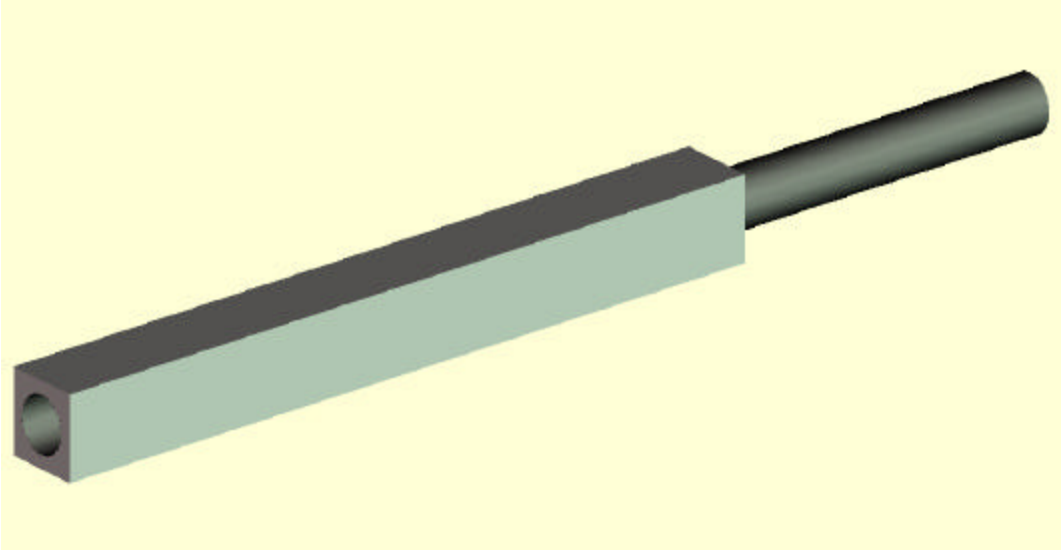


Figure 43 - Bored out graphite foam adhesively bonded to inner carbon/epoxy shell

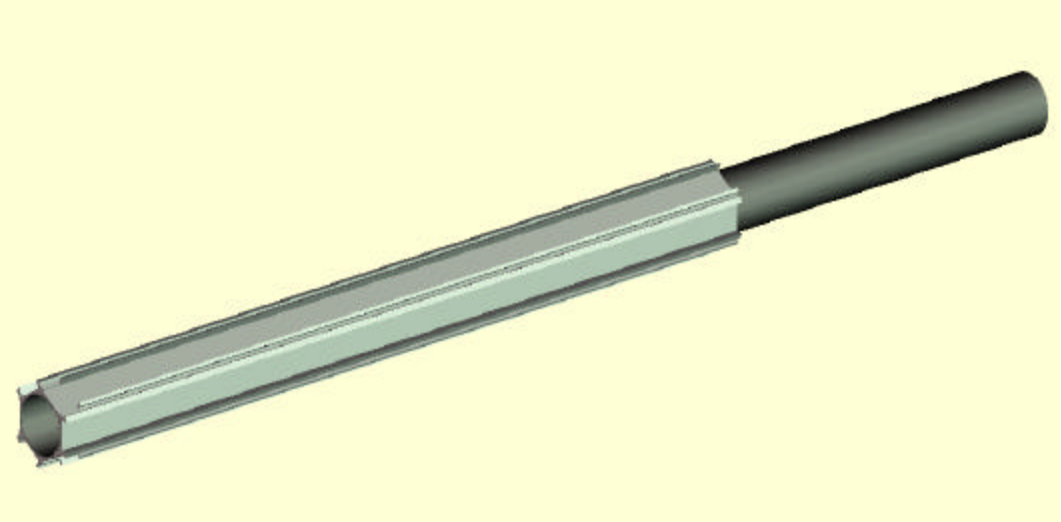


Figure 44 - Machined graphite foam on inner carbon/epoxy shell

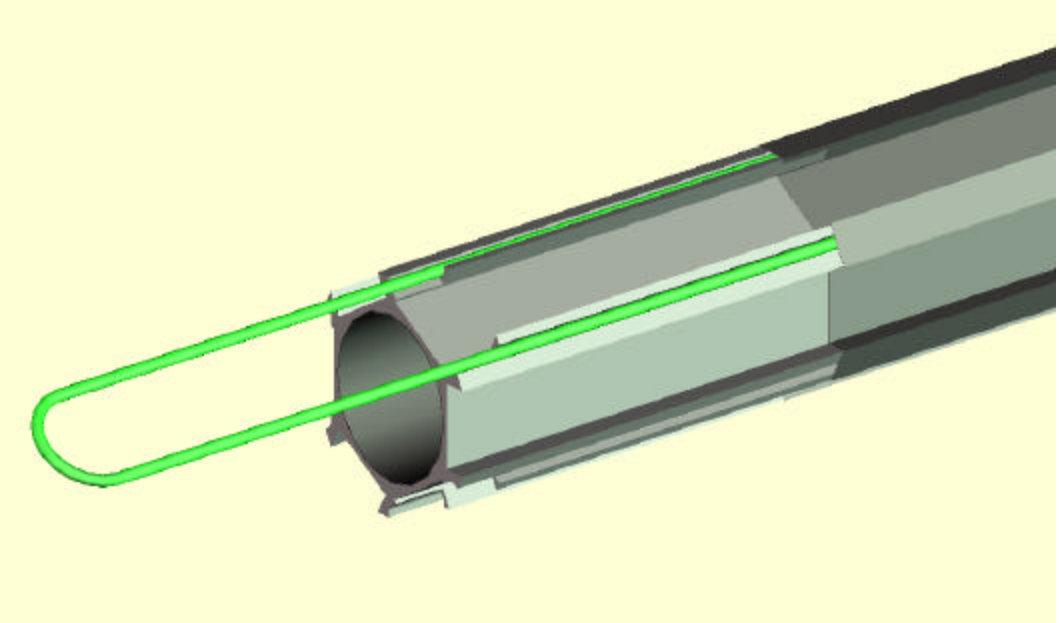


Figure 45 - Coolant tube and outer carbon/epoxy shell slide on to Figure 44 assembly

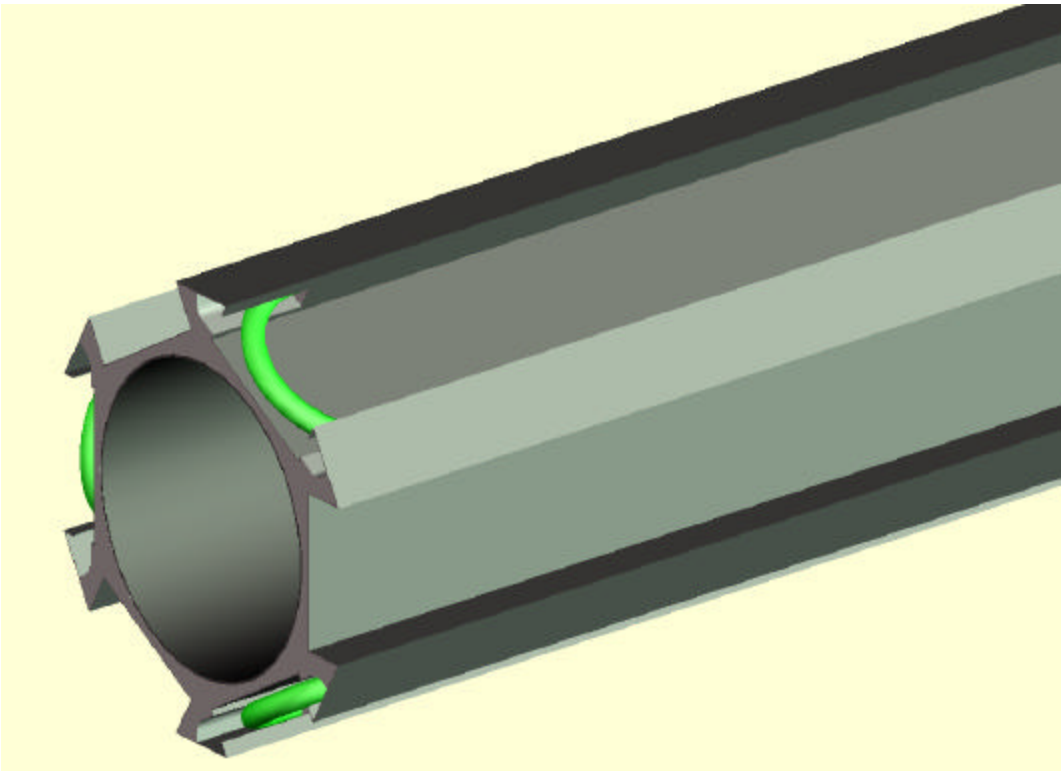


Figure 46 - Finished assembly

Although the manufacturing and assembly processes described above may appear to be straightforward, in reality there are many challenging manufacturing difficulties. Among the most prominent are as follows:

1. If the outer shell is produced using unidirectional pre-preg, then assuring high quality during lay-up of the θ bias plies will be difficult. Presumably, the bias plies will be created using strips of unidirectional pre-preg applied in a helical pattern around the periphery of the castellated tool shown in Figure 40. Maintaining a constant fiber angle as the pre-preg is laid along the castellated surface of the tool will be difficult, and will likely require special fixtures to insure constant fiber orientation along the length of the outer shell. In this regard it is probable that a constant bias fiber angle will be easier to maintain if the use of a braided tubular fiber preform and the RTM process proves to be a viable option.

2. Incorporating bonding of the annealed pyrolytic graphite film to the outer surface of the carbon/epoxy shell with cure of the pre-preg system may prove to be difficult. If so, then the graphite film will be bonded to the outer surface following cure of the carbon/epoxy shell, prior to bonding of the kapton film. This would likely require a second set of molds.

3. The graphite foam being considered for use was developed in recent years. Very little manufacturing experience with this product is available. Samples received to date have been porous and somewhat brittle. It is not clear that this material can be ground to the shapes implied in Figure 44, especially given the tolerances required. Also, due to the porous nature of this material an excessive amount of liquidous adhesive may wick into the foam due to capillary action during any step involving adhesive bonding, such as those implied in Figure 42, 43, 45, and 46, for example. If this proves to be a problem it may be possible to seal the surface of the graphite foam prior to final bonding, but this possibility has not yet been demonstrated.

4. The outer carbon/epoxy shell will be slid over the inner shell/graphite core/cooling tube during assembly (Figure 45,46). It may be difficult to hold the tolerances involved such that this can be accomplished without damage to the graphite foam core.

5.3.5 Layer 0-1 mechanical supports and connections

The connections between L0 and L1 and between L1 and the L2-L5 support structure must allow for simple assembly and removal while also providing the required high precision locations of these sub-assemblies with respect to the L2-L5 assembly. The L2-L5 staves use precision pins and sockets to achieve similar goals. It is proposed to use the same or similar components for L0-L1. The actual precise location of the pins and sockets may be obtained either by construction or by precise placement and fixing in position using a CMM. Connections will be made at Z=0 and Z=600 cm.

a) Z=0

The design concept consists of two circular carbon fiber/epoxy membranes, one attached to each of L0 and L1. The L0 membrane is glued to the end of the carbon fiber inner tube of the L0 assembly. It has three pockets, each of which contains a precision pin as seen in Figure 47 below.

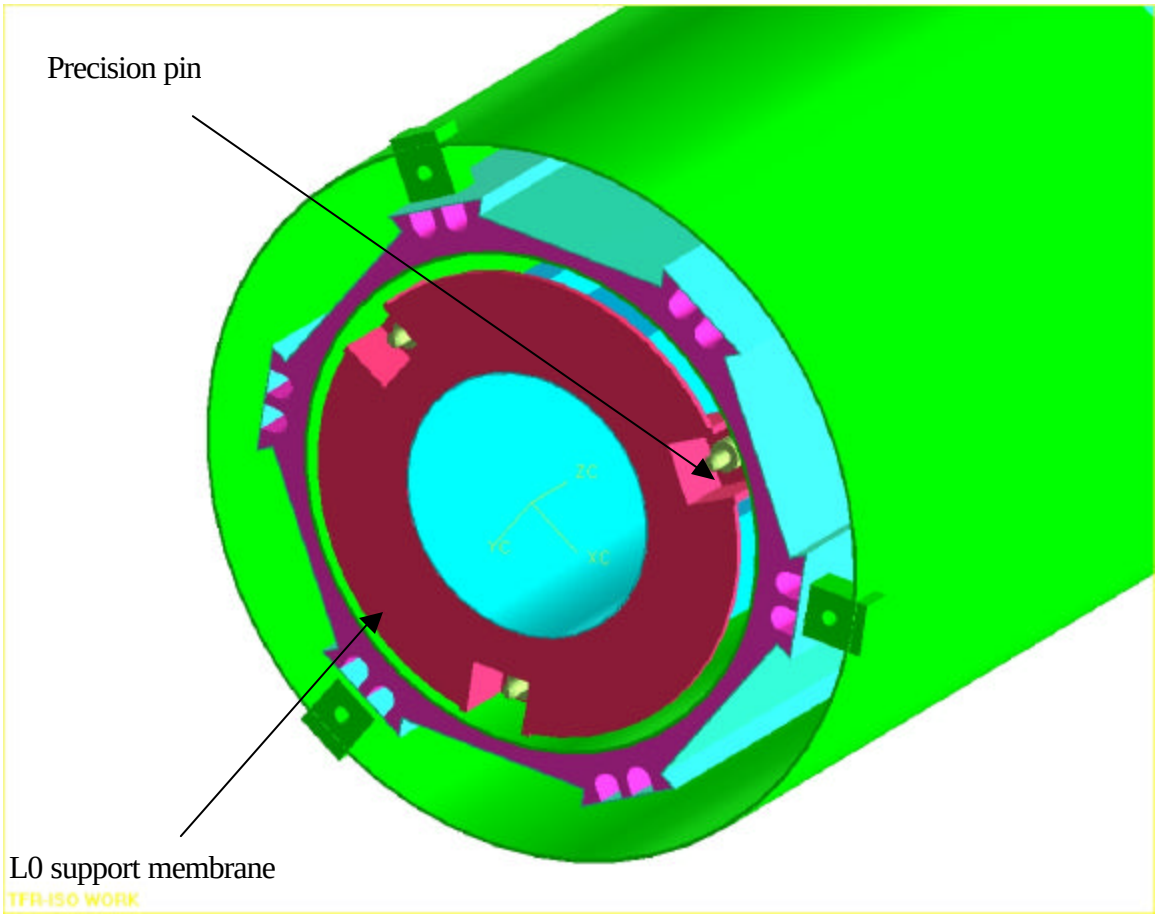


Figure 47 - L0 support membrane

L1 has a similar membrane (Figure 48), this having precision sockets at its inner edge that engage with the pins on the L0 membrane. It also has a set of pockets at its outer edge. These have precision pins that engage with sockets on the inner surface of the L2-L5 structure. This membrane is glued to the end of the L1 inner carbon fiber tube.

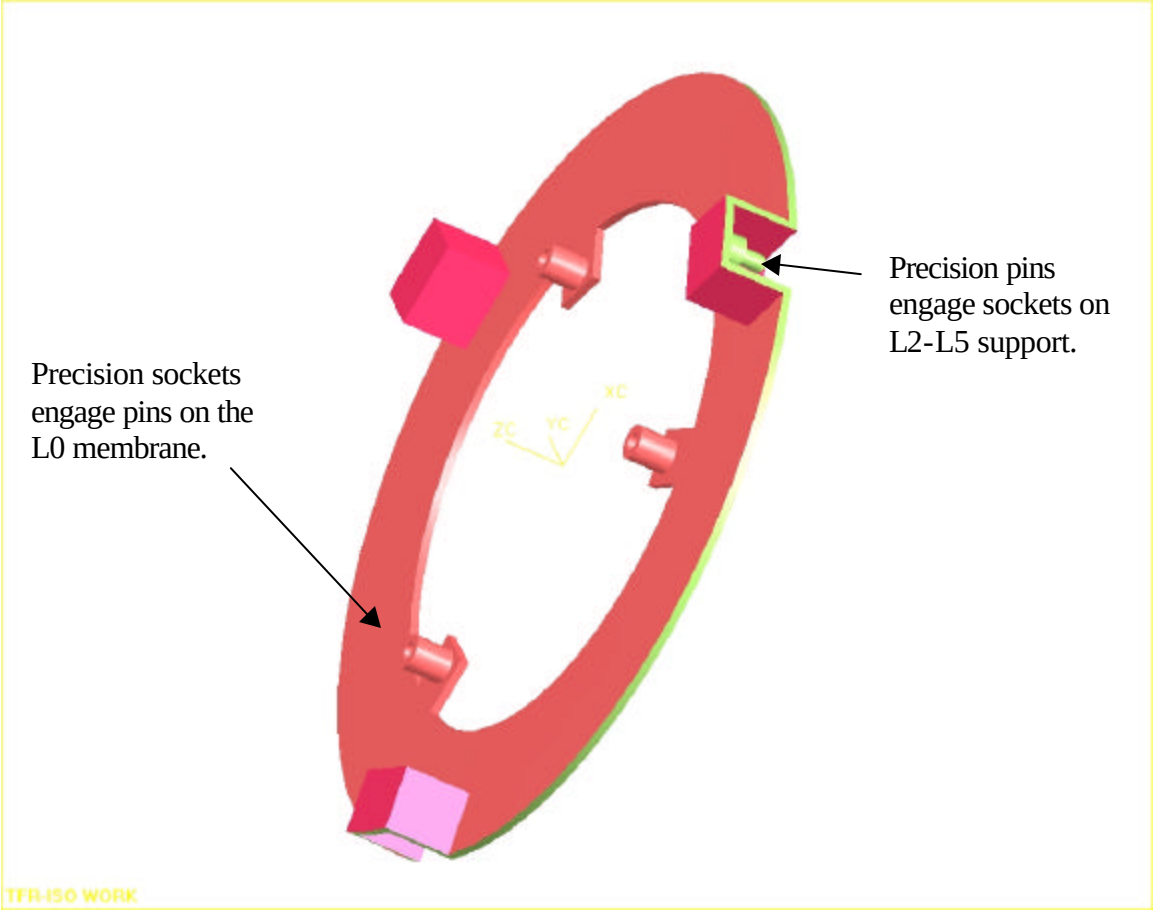


Figure 48 - L1 support membrane at Z=0.

The sockets on L2-L5 are shown schematically in Figure 49 and the whole assembly is seen in Figure 50.

The above design uses two membranes. This was chosen over connecting both L0 and L1 to a single membrane, as the latter requires using more space in the Z direction. However, it may be possible to achieve to the required mounting precision with a single membrane. This issue will be resolved after further study.

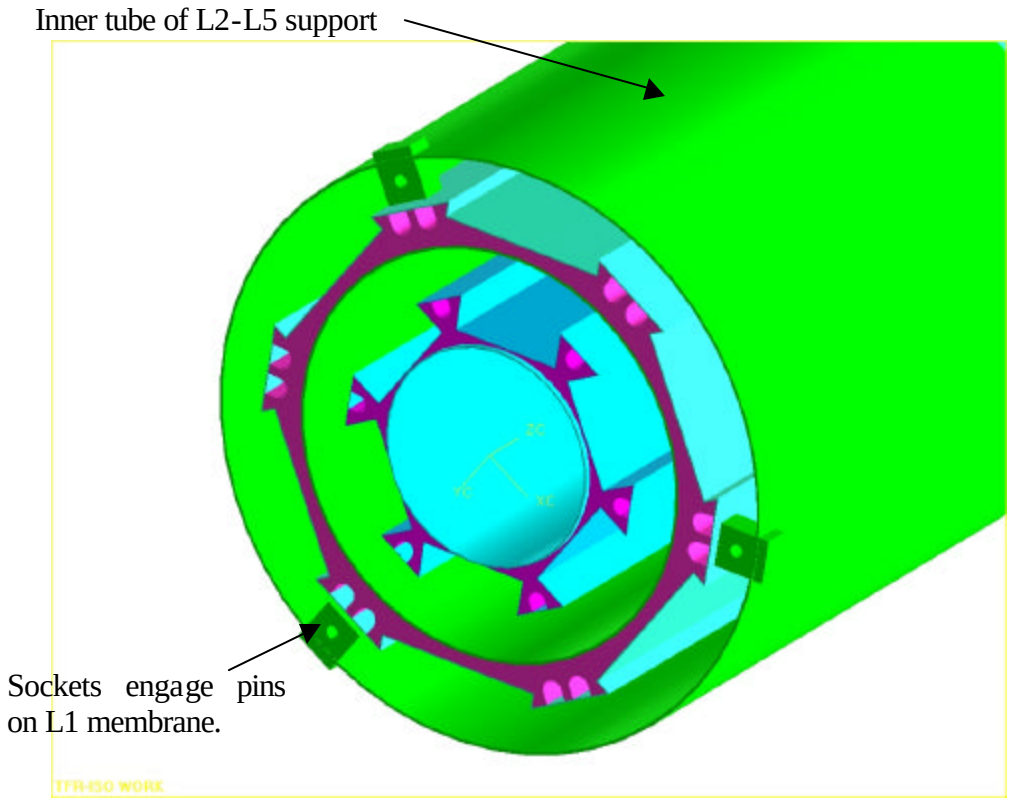


Figure 49 - Sockets on the L2-L5 support.

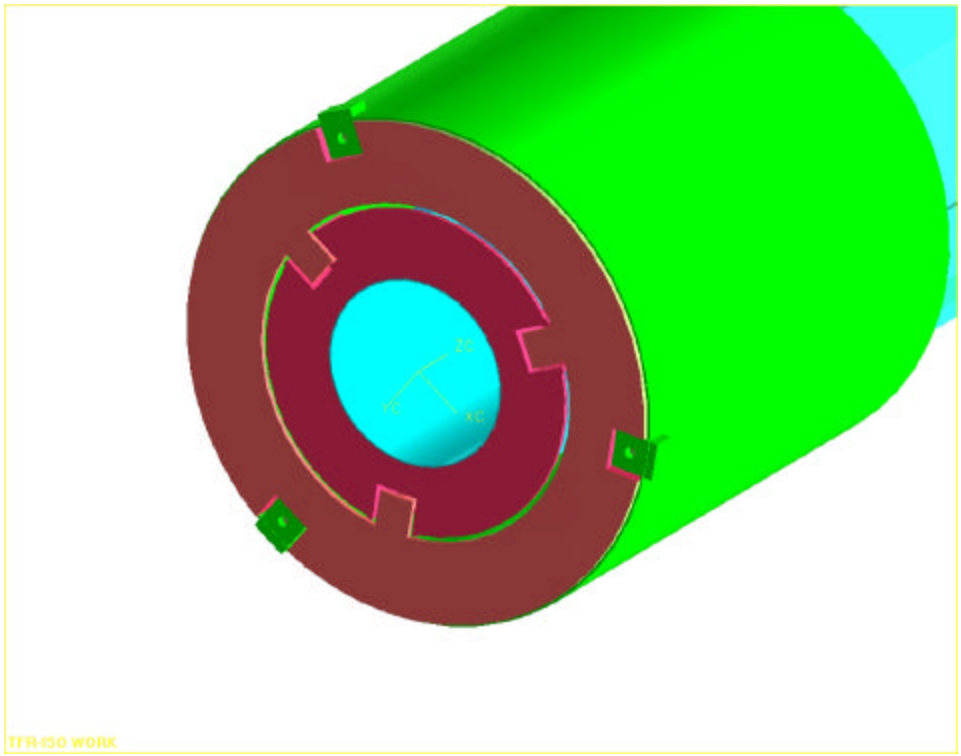


Figure 50 - L0/L1 support membranes at Z=0.

b) Z=600 mm:

At the outer end of the L0/L1 structure, the connection between L0 and L1 is complicated by the limited space available between the surfaces of the hybrid support stiffeners and the inner surface of L1. There is only 3.5 mm radial clearance and the digital cables coming from the L0b hybrids occupy much of this space. With that caveat, the design concept presented here is similar to that used at Z=0. Small blocks are attached to the outer surface of three of the hybrid support strips as seen in Figure 51.

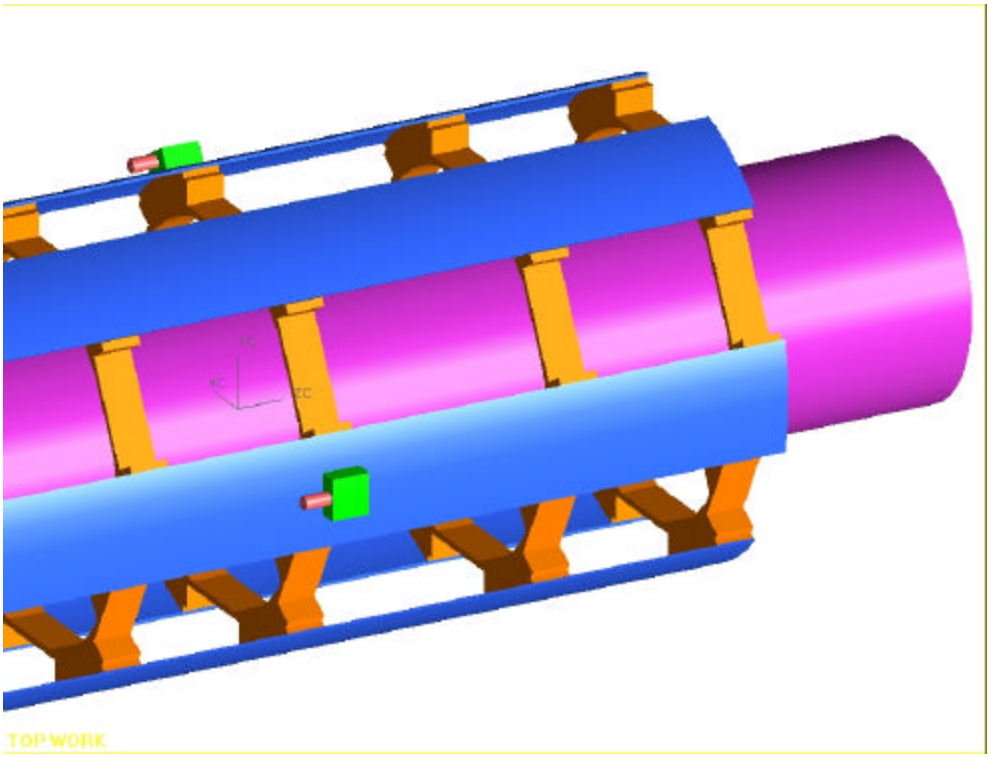


Figure 51 - Location pins and blocks on L0 structure at Z = 600 mm.

These pins mate with precise sockets on the inner surface of the L1 carbon fiber/epoxy tube as seen in Figure 52 and 53.

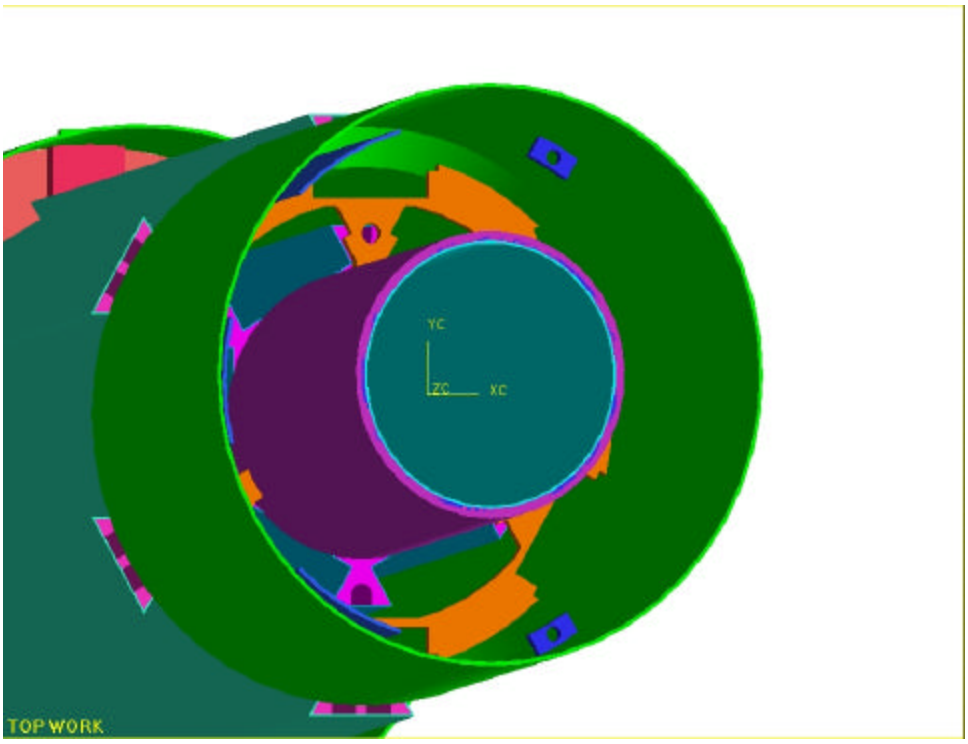


Figure 52 - Location blocks on inner surface of L1 carbon tube.

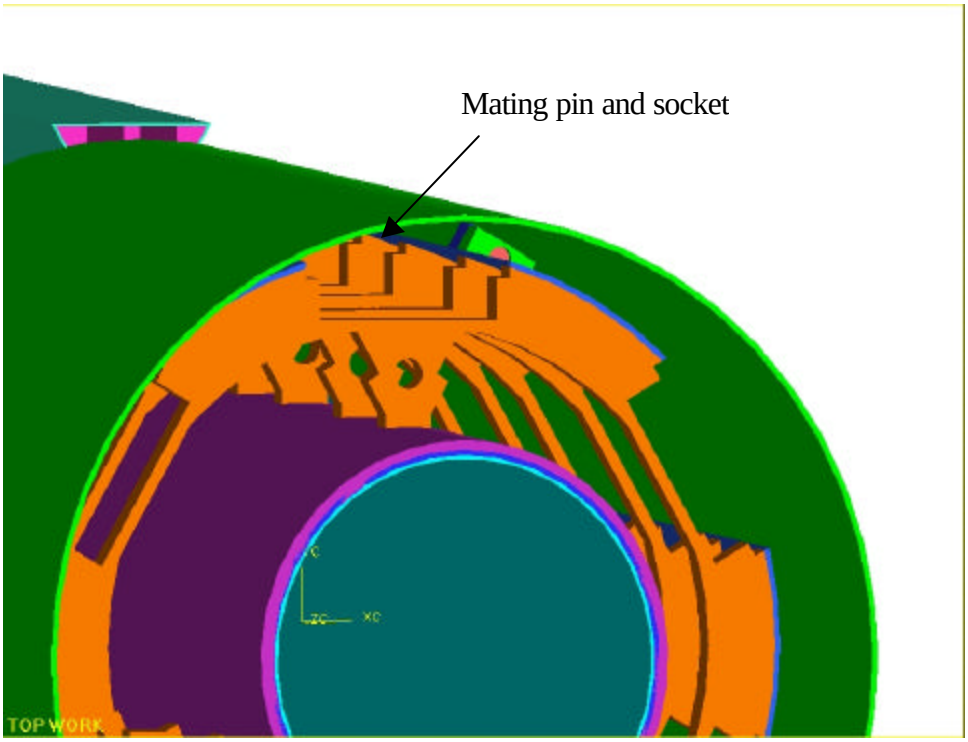


Figure 53 - L0 pins mate with L1 blocks and sockets.

The above pins and sockets must be positioned very precisely. This will need to be accomplished using a combination of precise jigging and CMM machines. In addition, an assembly jig will be needed to control the position of the delicate L0 assembly within L1 as the two are coupled together. Finally, the L0/L1 assembly will be held together by a spring/clamp at the outer end to keep the precision locating surfaces together.

The connection of the outer surface of L1 to the L2/L5 support structure is simpler to accomplish. An external support ring with three connection tabs is attached to the outer surface of L1 as seen in Figure 54.

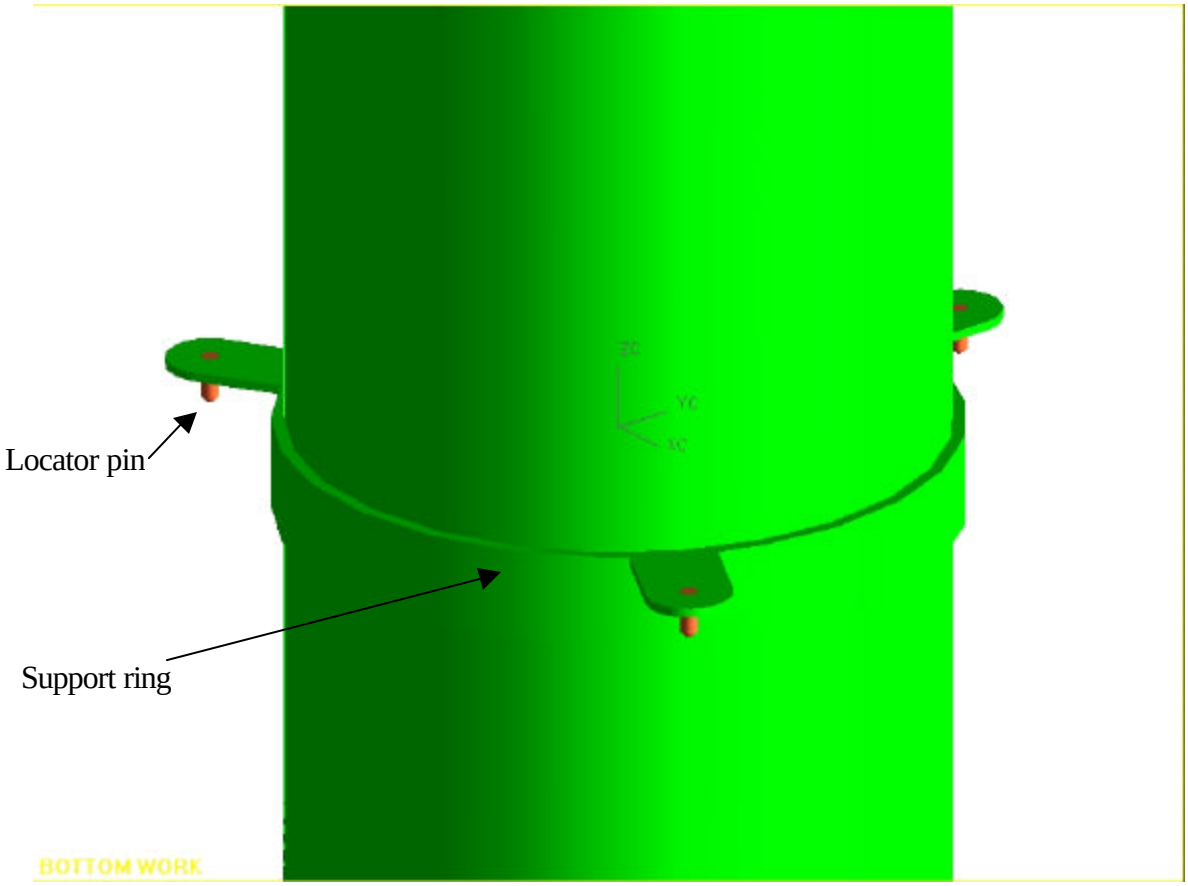


Figure 54 - External ring with tabs and locator pins attached to outside of L1.

Each tab has a precision pin which, in turn, locates into a precise socket in the end membrane of the L2/L5 support cylinder at Z = 600 mm as seen on Figure 55. The L2/L5 support is just shown in outline. Note that the support tabs have to be located on azimuth such that they come in between the ends of the inner ring of L2 staves. Again, a spring clip will be needed to keep the L0/L1 assembly against its Z position stop.

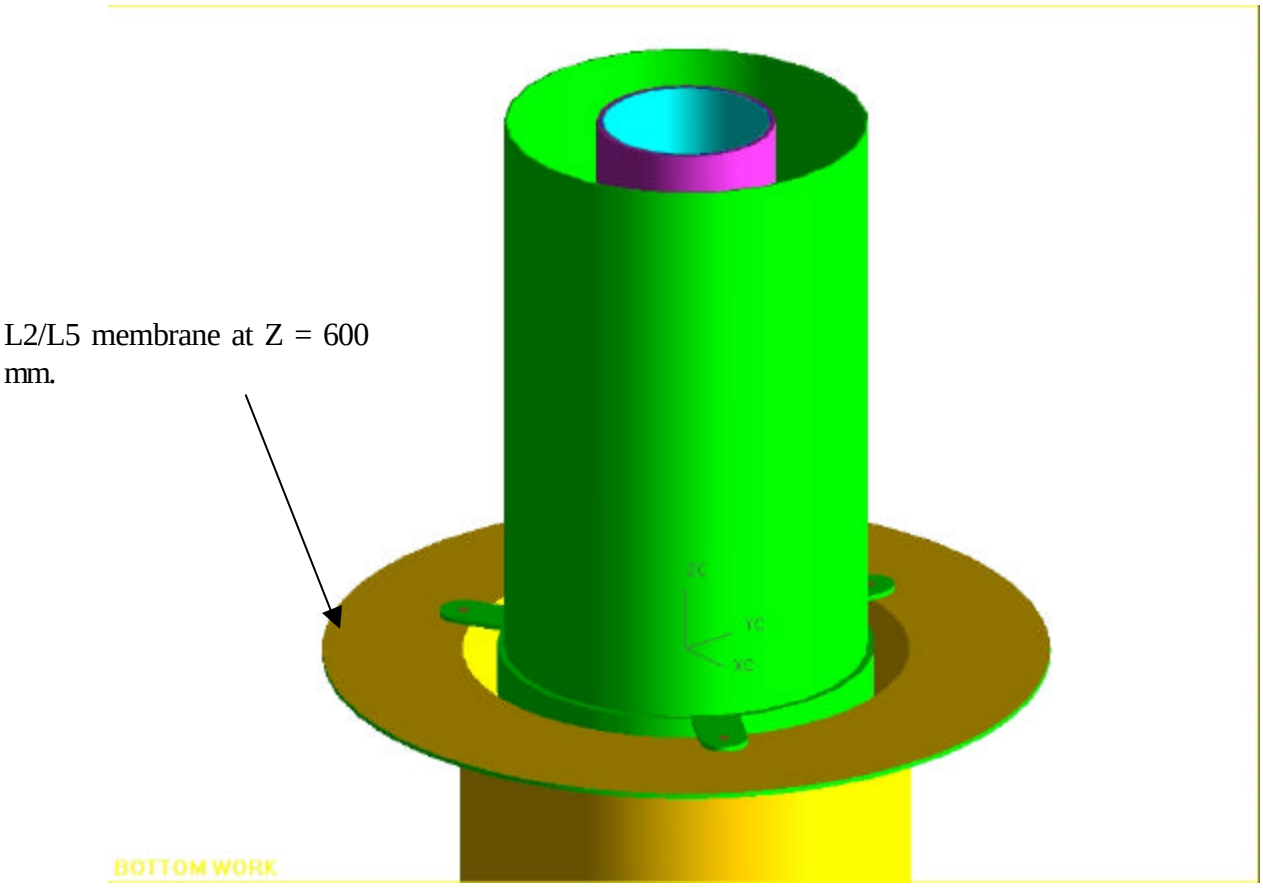


Figure 55 - L1 support tabs and pins connect to end of L2/L5 membrane.

To insert the L0/L1 assembly into the L2/L5 support, the inner end will be guided by the outer rim of the L1 support membrane at the Z = 0 end. Unless the outer ring of silicon and hybrids on L1 is protected, an insertion tool will be needed to guide L0 into L1. This should be designed so as to allow extraction/insertion of L0/L1 from the detector without having to remove L2/L5. This will be done via the access available from the central opening in the coolant bulkheads.

5.3.6 Appendix 5.3.A

Radiation Length Calculation for L0 in the Tracking Volume

L0 Items in central region (-480 < Z <480 mm)	Material	X_0 (mm)	L (mm) per sensor	Effective W (mm)	Effective t (mm)	Phi overlap correction	Average % of X_0	Subtotal % of X_0	X_0 %	Density (g/cc)	Weight (g) per sensor	Weight Fraction
Silicon								**0.46**	**28.4%**			**16.9%**
L0A silicon sensor at r = 18.5 mm	Si	94.0	80.0	15.5	0.300	0.80	0.255			2.33	0.867	16.9%
L0B silicon sensor at r = 24.5 mm	Si	94.0	80.0	15.5	0.300	0.60	0.193					
Expoy layer under silicon sensor	Epoxy	350.0	80.0	12.0	0.050	1.00	0.014					
Analog cable								**0.24**	**14.5%**			**17.2%**
L0A analog cable Kapton	Kapton	284.0	80.0	15.0	0.250	0.72	0.063			2.42	0.726	14.1%
L0A analog cable copper	Cu	14.0	80.0	3.0	0.025	0.14	0.026			8.94	0.054	1.0%
L0A analog cable gold	Gold	3.0	80.0	3.0	0.005	0.14	0.024			21.00	0.025	0.5%
Cable strain releave+wire bond protection	BeO	133.0	6.0	15.5	0.300	0.74	0.013			2.90	0.081	1.6%
L0B analog cable Kapton	Kapton	284.0	80.0	15.0	0.250	0.55	0.049					
L0B analog cable copper	Cu	14.3	80.0	3.0	0.025	0.11	0.019					
L0B analog cable gold	Gold	3.0	80.0	3.0	0.005	0.11	0.018					
Cable strain releave+wire bond protection	BeO	133.0	6.0	15.5	0.750	0.57	0.024					
HV insulation								**0.06**	**3.4%**			**5.3%**
Castellated Kapton shell (2 x 25 micron)	Kapton	284.0	80.0	19.0	0.050	1.73	0.030			2.42	0.184	3.6%
Epoxy (structural, 2x25 micron)	Epoxy	350.0	80.0	19.0	0.050	1.73	0.025			1.15	0.087	1.7%
Cooling								**0.08**	**4.8%**			**10.1%**
Peek tube (2.5mm OD, 0.10mm wall)	PEEK	350.0	80.0	7.9	0.100	0.33	0.009			1.30	0.082	1.6%
Coolant (converts to rectangular tube)	40% EG	358.0	80.0	2.3	1.806	0.10	0.048			1.00	0.332	6.5%
Thermal grease or graphite loaded epoxy	Epoxy	250.0	80.0	8.5	0.100	0.35	0.014			1.50	0.102	2.0%
Platinum resistor (4 on each side)	Varias	100.0	0.7	1.0	1.000	0.03	0.000			2.42	0.002	0.0%
Temperature sensor cable (AWG32)	Cu	14.3	80.0	0.18	0.180	0.005	0.006					
Mechanical support								**0.80**	**48.9%**			**79.1%**
Inner skin, 0.25 mm thick at r = 17mm	CF/epoxy	250.0	80.0	8.9	0.250	1.00	0.100			1.54	0.274	5.3%
Pyrolistic graphite sheet	Carbon	438.0	80.0	9.1	0.100	1.00	0.023			1.00	0.072	27.6%
Epoxy (0.05 mm for gluing graphite sheet)	Epoxy	250.0	60.0	9.1	0.050	1.00	0.015			1.15	0.031	3.0%
Castellated shell, 0.45 mm thick	CF/epoxy	250.0	80.0	19.0	0.450	1.73	0.312			1.54	1.053	20.5%
Epoxy (2x0.10 mm)	Epoxy	250.0	60.0	19.0	0.200	1.73	0.104			1.15	0.262	5.1%
Graphite foam core 0.2g/cc @ r = 21 mm	Carbon	2190.2	80.0	11.0	3.886	1.00	0.177			0.20	0.684	13.3%
Pyrolistic graphite sheet	Carbon	438.0	80.0	19.0	0.100	1.73	0.040			1.00	0.152	3.0%
Epoxy (0.05 mm for gluing graphite sheet)	Epoxy	250.0	60.0	19.0	0.050	1.73	0.026			1.15	0.066	1.3%
					Summary		**Total X_0 (%)**	**1.63**		**Weight=**	**5.136**	**g/sensor**

Appendix 5.3.A (cont'd)

Radiation Length Calculation for L1 in the Tracking Volume

L1 Items in central region (-480 < Z <480 mm)	Material	X_0 (mm)	L (mm) per sensor	Effective W (mm)	Effective t (mm)	Phi overlap correction	Average % of X_0	Subtotal % of X_0	X_0 %	Density (g/cc)	Weight (g) per sensor	Weight Fraction
Silicon								**0.43**	**17.7%**			**12.7%**
L1A silicon sensor at r = 35.0 mm	Si	94.0	80.0	25.0	0.300	0.68	0.218			2.33	1.398	12.7%
L1B silicon sensor at r = 39.2 mm	Si	94.0	80.0	25.0	0.300	0.61	0.194					
Expoy layer under silicon sensor	Epoxy	350.0	80.0	20.0	0.050	1.03	0.015					
Hybrid+digital+HV Cable+T-sensor								**0.94**	**39.1%**			**35.0%**
L1A hybrid (average = 1.2% r.l.)	Varies	83.3	22.5	25.5	1.000	0.68	0.230			5.00	1.867	17.0%
L1A digital cable, 0.25 mm kapton	Kapton	284.0	80.0	14.0	0.333	0.36	0.042			2.42	0.903	8.2%
L1A digital cable, 0.05 mm aluminum	Aluminum	89.0	80.0	14.0	0.067	0.36	0.027			2.42	0.181	1.6%
L1A digital copper, 0.0079g/cm2	Cu	14.3	80.0	10.5	0.090	0.27	0.171			8.90	0.673	6.1%
L1A HV cable Kapton	Kapton	284.0	80.0	3.0	0.267	0.08	0.008			2.42	0.155	1.4%
L1B HV cable copper, 0.0079g/cm2	Cu	14.3	80.0	1.0	0.090	0.03	0.017			8.90	0.064	0.6%
L1B hybrid (average = 1.2% r.l.)	Varies	83.3	22.5	25.5	1.000	0.61	0.206					
L1B digital cable, 0.25 mm kapton	Kapton	284.0	80.0	14.0	0.333	0.34	0.040					
L1B digital cable, 0.05 mm aluminum	Aluminum	89.0	80.0	14.0	0.067	0.36	0.027					
L1B digital copper, 0.0079g/cm2	Cu	14.0	80.0	10.5	0.090	0.24	0.154					
L1B HV cable Kapton	Kapton	284.0	80.0	3.0	0.267	0.07	0.007					
L1B HV cable copper, 0.0079g/cm2	Cu	14.3	80.0	1.0	0.090	0.02	0.015					
HV insulation								**0.04**	**1.6%**			**2.5%**
Castellated Kapton shell (2 x 25 micron)	Kapton	284.0	80.0	19.0	0.050	1.19	0.021			2.42	0.184	1.7%
Epoxy (structural, 2x25 micron)	Epoxy	350.0	80.0	19.0	0.050	1.19	0.017			1.15	0.087	0.8%
Cooling								**0.11**	**4.7%**			**6.2%**
PEEK tube (3.2mm OD, 0.10mm wall)	PEEK	350.0	80.0	10.0	0.100	0.51	0.014			1.30	0.104	1.0%
Coolant (converts to rectangular tube)	40% EG	358.0	80.0	3.0	1.806	0.15	0.076			1.00	0.433	4.0%
Thermal grease or graphite loaded epoxy	Epoxy	250.0	80.0	10.0	0.100	0.42	0.017			1.50	0.121	1.1%
Platinum resistor (4 on each side)	Varies	100.0	0.7	1.0	1.000	0.02	0.000			2.42	0.002	0.0%
Temperature sensor cable (AWG32)	Cu	14.3	80.0	0.18	0.180	0.005	0.006			8.90	0.023	0.2%
Mechanical support								**0.69**	**28.7%**			**93.6%**
Inner skin, 0.30 mm thick at r = 32 mm	CF/epoxy	250.0	80.0	16.7	0.400	1.00	0.160			1.54	0.825	7.5%
Pyrolistic graphite sheet at r = 32.5 mm	Carbon	438.0	80.0	17.0	0.100	1.00	0.023			1.00	0.136	52.6%
Epoxy (0.05 mm for gluing graphite sheet)	Epoxy	250.0	60.0	17.0	0.050	1.00	0.015			1.15	0.059	4.2%
Castellated shell, 0.45 mm thick	CF/epoxy	250.0	80.0	25.0	0.450	1.19	0.214			1.54	1.386	12.6%
Epoxy (2x75 microns)	Epoxy	250.0	60.0	25.0	0.150	1.19	0.053			1.15	0.259	2.4%
Graphite foam core 0.2g/cc @ r = 37mm	Carbon	2190.2	80.0	20.0	4.000	1.00	0.183			0.20	1.280	11.7%
Pyrolistic graphite sheet	Carbon	438.0	80.0	25.0	0.100	1.19	0.027			1.00	0.200	1.8%
Epoxy (0.05 mm for gluing graphite sheet)	Epoxy	250.0	60.0	25.0	0.050	1.19	0.018			1.15	0.086	0.8%
L1 outer shell								**0.20**	**8.3%**			
L1 outer shell (optinal) at r = ~45 mm	CF	250.0	35.0	20.0	0.500	1.00	0.200			1.54	0.539	4.9%
					Summary		**Total X_0 (%)**	**2.42**		**Weight=**	**10.965**	**g/sensor**

Appendix 5.3.A (cont'd)

Radiation Length Calculation for L0/L1 Assembly in the L0 Hybrid Region

L0/L1 Items in end region (~490 < |Z| < ~700 mm)	Material	X_0 (mm)	L (mm) per sensor	Effective W (mm)	Effective t (mm)	Phi overlap correction	Average % of X_0	Subtotal % of X_0	X_0 %	Density (g/cc)	Weight (g) per sensor	Weight Fraction
L0 analog cable								**0.24**	**5.3%**			
L0 Hybrid (35 mm z-pitch) and cable								**2.51**	**56.7%**			**37.6%**
L0A hybrid (average = 1.2% r.l.)	Varies	83.3	30.0	18.0	1.000	0.72	0.737			5.00	2.700	29.3%
L0A digital cable, 0.25 mm kapton	Kapton	284.0	35.0	14.0	0.333	0.54	0.063			2.42	0.395	4.3%
L0A digital cable, 0.05 mm aluminum	Aluminum	89.0	35.0	14.0	0.067	0.54	0.040			2.42	0.079	0.9%
L0A digital copper, 0.0079g/cm2 Cu	Cu	14.0	35.0	10.5	0.090	0.54	0.344			8.90	0.294	3.2%
L0B hybrid (average = 1.2% r.l.)	Varies	83.3	30.0	18.0	1.000	0.55	0.562					
L0B digital cable, 0.25 mm kapton	Kapton	284.0	35.0	14.0	0.333	0.42	0.050					
L0B digital cable, 0.05 mm aluminum	Aluminum	89.0	35.0	14.0	0.067	0.42	0.032					
L0B digital cable, 0.0079g/cm2 Cu	Cu	14.0	35.0	10.5	0.090	0.42	0.273					**9.9%**
L1 digital cable, 0.25 mm kapton	Kapton	284.0	35.0	14.0	0.250	0.62	0.055			2.42	0.296	3.2%
L1 digital cable, 0.05 mm aluminum	Aluminum	89.0	35.0	14.0	0.050	0.62	0.035			8.90	0.218	2.4%
L1 digital cable, 0.0079g/cm2 Cu	Cu	14.0	35.0	10.5	0.089	0.47	0.296			8.90	0.290	3.1%
L1 HV cable Kapton	Kapton	284.0	35.0	3.0	0.267	0.07	0.006			2.42	0.068	0.7%
L1 HV cable copper, 0.0079g/cm2	Cu	14.3	35.0	1.0	0.090	0.02	0.014			8.90	0.028	0.3%
Temperature sensor cable (AWG32)	Cu	14.3	35.0	0.18	0.180	0.003	0.003			8.90	0.010	0.1%
Hybrid support rings								**0.75**	**16.9%**			**22.8%**
Rings (1 mm Al struccture 10 mm thick)	Aluminum	89.0	10.0	78.0	1.000	2.33	0.748			2.70	2.106	22.8%
Cooling								**0.18**	**4.0%**			**6.1%**
L0 Peek tube (2.5mm OD, 0.10mm wall)	PEEK	350.0	35.0	7.9	0.100	0.33	0.009			1.30	0.036	0.4%
L0 coolant (converts to rectangular tube)	40% EG	358.0	35.0	2.3	1.806	0.10	0.048			1.00	0.145	1.6%
L0 cooling tube protection	PEEK	350.0	35.0	7.9	0.200	0.33	0.019			1.30	0.071	0.8%
L1 PEEK tube (3.2mm OD, 0.10mm wall)	PEEK	350.0	35.0	10.0	0.100	0.51	0.014			1.30	0.046	0.5%
L1 coolant (converts to rectangular tube)	40% EG	358.0	35.0	3.0	1.806	0.15	0.076			1.00	0.190	2.1%
L1 cooling tube protection	PEEK	350.0	35.0	7.9	0.200	0.20	0.011			1.30	0.071	0.8%
Mechanical support								**0.56**	**12.6%**			**16.8%**
Inner L0 skin, 0.50 mm thick at r=17mm	CF/epoxy	250.0	35.0	20.0	0.500	1.00	0.200			1.54	0.539	5.8%
Inner L1 skin, 0.75 mm thick at r=35 mm	CF/epoxy	250.0	35.0	25.0	0.750	1.19	0.356			1.54	1.011	11.0%
L1 outer shell								**0.20**	**4.5%**			**6.9%**
L1 outer shell (optinal) at r = ~45 mm	CF/epoxy	250.0	35.0	23.6	0.500	1.00	0.200			1.54	0.635	6.9%
					Summary	**Total X_0 (%)**		**4.43**		**Weight=**	**9.229**	**g/sensor**

5.4 Layer 2-5 Mechanical Design

The outer four layers of the tracker consist of 168 staves, 84 in each sub-barrel. Each stave contains four silicon modules, two axial and two small angle stereo. The stave provides active cooling to remove the heat generated by the readout electronics and the sensors, maintains the planarity of the silicon sensors, and provides for the accurate alignment of the sensor planes in space.

5.4.1 Readout configuration

The azimuthal multiplicity of each sensor layer must be divisible by 6 in order to fit in the existing silicon track trigger. Although not a hard constraint, we felt it very desirable to limit the number of sensor and hybrid types, our goal being only one sensor type for all four outer layers. This leads to ϕ segmentation of 12, 18, 24 and 30 in layers 2, 3, 4 and 5, respectively. Given the radii of these layers (≈50-160mm) the necessary sensor active width is determined to be 32-38mm. We wish to produce two sensors per 6" silicon wafer, so the length of the sensors is limited to ~110mm. To obtain the desired η coverage, layers 2-3 should have 500mm of sensor coverage while layers 4-5 should have 600mm of coverage (each side of z=0). This leads to a natural choice of 100mm for the sensor length.

The readout cable plant is limited to about 912 by the existing electronics. Of these, roughly 200 need to be reserved for the inner two layers of the tracker. Dead time considerations limit the total number of SVX channels that can be accommodated on one readout cable; this limit is 10 chips for layers 2-5. The available cable plant cannot accommodate fine pitch (50-60 μm) readout with fine (100 mm) z-segmentation. Simulations of resolutions, pattern recognition and occupancy found a substantial preference for finer pitch over finer z segmentation. In addition, finer pitch also allows for direct wire bonding from the SVX chips to the sensors. We have chosen a sensor design with 640-channels at 60 μm pitch, for an active width of 38.4 mm.

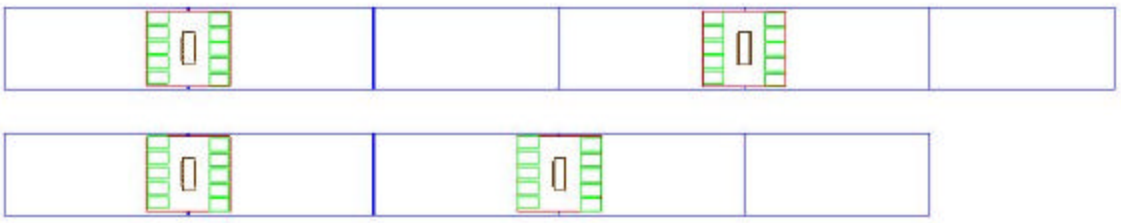


Figure 56: Readout configuration for outer layer staves. The upper configuration is for layers 4 and 5 and the lower is for layers 2 and 3. The axial sensors are shown.

The outer layers contain staves five sensors long in layers 2-3 and six sensors long in layers 4-5 (Figure 56). Closest to z=0, all staves have a 200 mm long module with two 100 mm readout segments. In layers 2-3, the second module is 300 mm long, with 100 mm readout towards z=0 and 200 mm readout at the end of the stave. In layers 4-5 the second module is 400 mm long with two 200 mm readout segments. To form the 200 mm readout segments, two 100 mm

sensors are glued end-to-end and electrically coupled with wirebonds on the top and a bias connection between the back planes.

5.4.2 Silicon modules

The outer layer silicon modules consist of two, three or four silicon sensors, each 100 mm in length by 41.1 mm in width, joined together with a single readout hybrid. The readout hybrid is double-ended, meaning that the hybrid straddles two sensors with separate SVX chips reading out the signals from each end (Figure 57).

There are a total of six types of modules labeled by the length in centimeters of the sensor read out. The same sensor and hybrid are used in all six of the module types. The three axial modules differ only in the number of sensors used, while the three stereo module types use different stereo angles depending on the lengths of the readout segments; 1.25 degrees for 200mm readout, 2.5 degrees for 100mm readout. While the larger stereo angle would be preferred throughout the device, tight geometrical constraints limit the width of the staves, and hence the maximum allowable stereo angle as a function of readout length. In the case of the 3-sensor long stereo modules (10/20 modules) used at the outer ends of layers 2-3 (Figure 57), the single sensor is at the end closer to z=0 with a 2.5 degree angle, while the two ganged sensors are oriented at a 1.25 degree stereo angle. For the 4-sensor modules used at the ends of the staves (20/20 modules) in layers 4-5, both ends have ganged sensors with 1.25 degree stereo angle. This arrangement provides 2.5 degree stereo coverage and 100mm readout segmentation for $|z|<300$ mm in layers 2-3 and $|z|<200$ mm in layers 4-5. The full coverage is $|z|<500$ mm in layers 2-3 and $|Z|<600$ mm in layers 4-5.

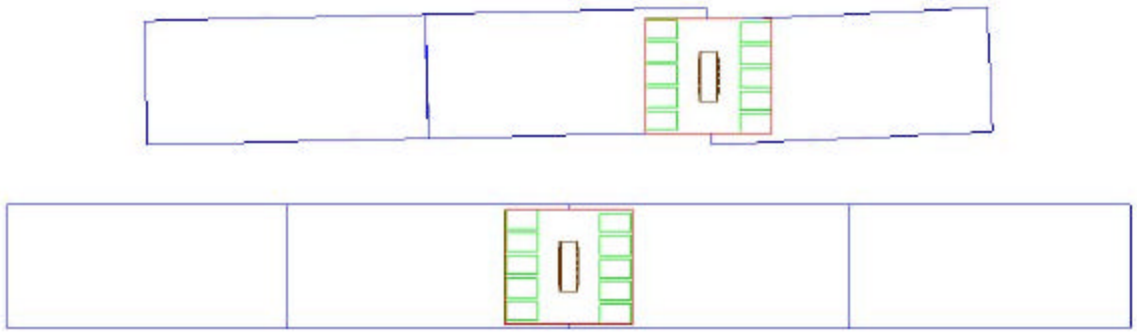


Figure 57: Module assemblies. Top: A three-sensor long small angle stereo module. Bottom: A four-sensor long axial module.

Each hybrid has 10 SVX chips, 5 at each end of their approximately 45mm length. Each SVX chip generates 0.3-0.5W of heat, with 50% of that heat load concentrated in narrow regions near the two ends of the chip. For design purposes we have assumed a 0.5W load per chip. A connector located at the center of the hybrid provides the power, control signals for the chips and

the high voltage for the sensor bias. A bias line wraps around the edge of the sensor to provide a connection directly to the back plane of the sensor.

The techniques for assembly of sensor modules are similar to those used in the past by many groups, including DØ. Sensors are manually aligned with optical feedback from a camera mounted on a coordinate measurement machine (CMM). Once aligned, the sensors are glued to one another, directly or via a connecting substrate. Reasonable expectations for this alignment are a few microns. The hybrid, previously assembled, burned-in and tested, is glued directly to the silicon sensors. Wire bonding is then done between the hybrid and the sensors, and from sensor to sensor for the modules with 200mm readout segments. The sensor pitch has been chosen so that the hybrid to sensor bonding can be done directly from the SVX chips to silicon sensors without a pitch adapter. The total numbers of wire bonds required for layers 2-5 are 353K sensor-to-sensor plus 860K hybrid-to-sensor, for a total of 1213K bonds. For the longer modules, the sensor-to-sensor wire bonding can be done either before or after the hybrid is mounted. Sensor alignment and sensor-to-sensor wire bonding can proceed prior to hybrid delivery, should that become a production constraint.

The completed module will undergo electrical testing, additional burn-in, and laser scanning, described elsewhere in this document, prior to assembly into staves.

5.4.3 Stave assemblies

The outer four layers of the silicon tracker are constructed as 168 staves, approximately 45mm wide by 8.9mm tall by 610mm in length (Figure 58). Each stave is independently mounted to a set of bulkheads, described previously. The stave structures consist of a core with silicon mounted to both surfaces and two external shells enclosing the silicon in a box-beam structure. The core structure has an integrated cooling circuit to remove the heat generated by both the hybrid electronics and the silicon sensors. The core also provides the precise reference features for aligning and mounting sensor modules to the core and the completed stave to the bulkheads. Finally, the core maintains the flatness of the silicon sensors. The external shells provide the necessary bending and torsional stiffness to the stave.

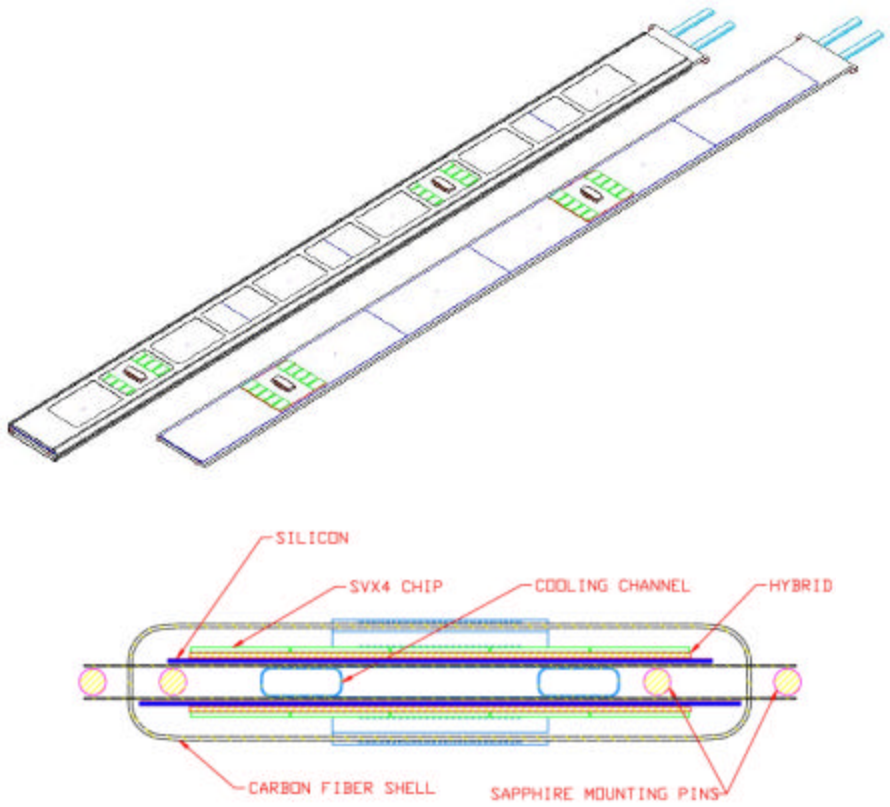


Figure 58: Stave assembly drawings. The upper drawing shows isometric views of the stave before and after installation of the outer shells. The lower plot is an end view of a complete stave assembly.

The core structure is about 3mm tall, consisting of two 150μ thick skins of high thermal conductivity carbon fiber (Mitsubishi K13C2U, K=620W/mK) coupled by a core material that carries the shear load between the skins. Two core materials are being evaluated – Rohacell foam and a carbon fiber honeycomb structure. Also embedded between the skins is a cooling passage made from 100μ wall PEEK tubing formed to a stadium shape profile with interior dimensions of roughly 6mm x 2mm. The cooling passage runs down the stave length about ¼ of the width from one edge, turns around near the Z=0 end of the stave and runs back out ¼ of the width from the opposite edge of the stave. The fluid dynamics, thermal performance and mechanical performance of this structure are described below. Precision mounting and alignment features - ruby and sapphire rods and spheres - are an integral part of the core structure. Once assembled, the core structure can be leak checked and inspected for dimensional tolerances prior to population with silicon modules.

The silicon modules are bonded directly to the stave core. The outer surfaces of the carbon fiber skins are electrically insulated from the back planes of the silicon sensors with 50μ of Kapton.

One side of the core is populated with axial sensor modules while the other is populated with small angle stereo modules. The mounting and reference features on the stave core are accessible from both sides of the stave so that they can be used to establish the reference system on a CMM for alignment of the silicon modules to the stave core. Past experience is that module-to-module alignment can be done at the sub-5μ level.

Carbon fiber shell structures mount over the silicon on each side, directly to the core structure. These structures provide most of the stiffness of the completed stave, provide a surface for the readout cables to attach to as they run to the end of the stave, and help to protect the sensors and hybrids from damage during further processing steps. These structures are 0.3-0.5mm thick with their outer surfaces spaced 8.9mm apart. Large cutouts in the shell structures reduce the mass of the structure and allow access for connecting the readout cables to the hybrids.

5.4.4 Stave mass and radiation length

The stave mass and radiation length have been estimated, with the hybrid mass scaled from previous experience. The stave weight per unit length is 2.3g/cm. The radiation length (Table 5), averaged over the silicon area, is just under 1.9%X_0 per layer. The breakdown of the material is 0.64%X_0 sensors, 0.35%X_0 hybrids, 0.34%X_0 readout cables, 0.14%X_0 coolant and tube, and 0.41%X_0 for the stave structure and adhesives. The equivalent of 1.5 readout cables are included in this estimate; the first cable begins at Z=100mm and the second at Z=300mm (400mm) in layers 2-3 (layers 4-5). A track passing at normal incidence through the hybrids sees roughly 3.9%X_0 per layer. Near Z=0, where there are no cables or hybrids, the radiation length is only 1.2%X_0 per layer.

Table 5 - Breakdown of stave radiation length by material. The table below is for the layer 4-5 staves.

Item	Material	X0 (cm)	L (mm)	W (mm)	t (mm)	%X0 (local)	%X0 (avg.)	Fraction
Silicon sensors	Si	9.4	600.0	41.4	0.600	0.638	0.638	**34.0%**
SVX4 chips	Si	9.4	36.0	32.0	0.720	0.766	0.036	
BeO substrate	BeO	13.3	90.0	38.4	0.760	0.571	0.080	
Hybrid Kapton	Kapton	28.4	90.0	38.4	0.200	0.070	0.010	
Hybrid metalization	Cu	1.4	90.0	38.4	0.044	0.314	0.044	
Epoxy, conductive	Loaded epoxy	10.0	36.0	38.4	0.200	0.200	0.011	
Surface mnt. comp.	High Z	1.0	37.6	11.0	0.500	5.000	0.083	
Solder	Pb/Sn	0.9	26.2	38.4	0.200	2.222	0.090	**18.8%**
Readout cable Kapton	Kapton	28.4	600.0	20.0	0.600	0.211	0.102	
Readout cable copper	Cu	1.4	600.0	14.0	0.096	0.686	0.232	**17.8%**
Peek tube	PEEK	35.0	600.0	12.7	0.236	0.067	0.021	
Coolant	40% EG	35.8	600.0	12.3	1.436	0.401	0.119	**7.4%**
Carbon fiber skins	CF	25.0	600.0	45.8	0.150	0.060	0.066	
Kapton insulator	Kapton	28.4	600.0	45.8	0.100	0.035	0.039	
Rohacell 51 foam	Rohacell 51	735.0	600.0	33.1	1.778	0.024	0.019	
Epoxy, conductive	Loaded epoxy	10.0	60.0	12.7	0.150	0.150	0.005	
Carbon fiber shells	CF	25.0	600.0	32.0	0.610	0.244	0.188	
Epoxy, structural	Epoxy	35.0	600.0	45.8	0.300	0.086	0.095	**22.0%**
Total							**1.878**	

5.4.5 Stave mechanical connection

The staves are mounted to a pair of bulkheads, located at Z=0 and Z=600mm, that are coupled to each other by carbon fiber tubes. The carbon fiber tubes have a coefficient of thermal expansion (CTE) very near zero, while the staves are expected to have a CTE of 1.5ppm/C. We anticipate the staves shrinking by roughly 30μ between assembly at room temperature and operation with –15C coolant (see Figure 60 in the section on stave thermal performance). In addition there may be some relative motion of the bulkheads, particularly longitudinally, during transportation and installation of the device. In the transverse direction the spacing between the mount points is ~50mm so the differential contraction of the stave and carbon fiber bulkheads is only expected to be 2-3μ. This is negligible and need not be considered in the mount design. Were the bulkheads fabricated in beryllium rather than carbon fiber this differential contraction would be 15μ and the mounts would need to be redesigned to allow for this.

In order to allow for longitudinal motion we intend to use mounts consisting of sapphire rods inserted into ruby orifices. These parts are commercially available with a tolerance range of ±5μ on the fit. The stave will have two pins located at the outer end that engage the outer bulkhead at either side of the stave along the stave mid-plane, and similarly at the Z=0 end two pins emerge from between the sensors to engage the Z=0 membrane. Two options are being studied for providing a longitudinal constraint. The first option is to provide a stop at the Z=0 end with a spring load applied from the Z=600mm end of the stave. The second option is to fix the Z=600mm end of the stave to the outer bulkhead, allowing the stave to retract from the Z=0 membrane during cool-down. A four-point mount is necessary since the staves do not have large torsional stiffness (θ/τ=1mrad/120g-mm) compared to their mass (140g) and width (40mm).

5.4.6 Alignment precision and stave mounts

The alignment requirements for the sensors are determined by the requirements of the impact parameter trigger. The trigger does not have the stereo sensor information so any misalignment of the axial sensors to the beam axis results in a degradation of the r-ϕ resolution at the trigger level. The intrinsic device resolution is ≈8μ.

The roll angle, i.e. rotation around an axis parallel to the beam line, does not affect trigger resolution, provided that it is known from survey. For a rotation in the plane of the sensors (yaw), the desired alignment tolerance is <10μ over a readout segment, or an angle of <50μrad. This results in an alignment tolerance of ±30μ over the full stave length. The pitch angle affects strips at the edges of the sensors, but not at the center. For a radial deviation dR at an angle ϕ from the center of the sensor, the transverse measurement error dX is given by dX=dR$\tan\phi$. The worst case is at the edges of the sensors where $\tan\phi$=0.27(0.11) in layer 2(5). This implies a radial positioning tolerance of ±110(285)μ over the length of a stave in layer 2(5). If the sensors are not held flat within the stave the effect is identical to that of the pitch angle. Here the length scale is 100mm, so the tolerance on the sensor flatness is of order 20μ. It is difficult to anticipate the degree of warping which the production sensors will have due stresses induced in manufacturing. Very flat vacuum fixtures will be used to hold the sensors flat during bonding to the core. The 3mm tall core structure with sensors on both sides provides a significant moment of inertia to constrain the sensors flat.

The tolerances on the pins and orifices intended for mounting the staves are sufficiently tight to permit a mounting system without adjustment, provided the orifices can be located in the bulkheads with high precision. This is considered to be feasible. We are investigating adjustable mounts as a second option.

5.4.7 Layer 2-5 stave thermal performance

The mechanical and thermal characteristics of the staves have been evaluated both analytically and using finite element analysis (FEA). The thermal design goal is a maximum silicon temperature of 0 degree C for the outer layers using a solution of 40% ethylene glycol (by volume) in water, delivered to the stave at a temperature of –15C. This will ensure that the sensor depletion voltage remains below 300V in layer 2 for $30fb^{-1}$. Mechanically, the stave deflection limit is 75μ under its own weight. This limit is somewhat stricter than one might naively impose based on sensor alignment to the beam axis, but it ensures that the natural frequency of the stave remains well above 60Hz. In addition, all stress levels should remain below failure levels for loads up to 10 times gravity to provide a safety factor of 2 during transportation from the Silicon Detector Center to the experimental hall. We have also studied various loading cases that might occur during stave assembly and installation to confirm that the stave design is sufficiently robust.

The stave cooling channel has been sized to operate below atmospheric pressure, hence the pressure drop in limited to ≈3psi. The total stave heat load is dominated by the hybrids that generate up to 20W, while the sensors are not expected to contribute more than 3W in layer 2 after $30fb^{-1}$ of exposure. The expected operating point for the stave is a flow rate of 0.175lpm resulting in a pressure drop of 2.1psi from inlet to outlet with a bulk temperature rise of 1.9C. The tube wall will operate roughly 4.9C above the bulk temperature locally under the hybrids. Figure 59 shows the result of a finite element analysis (FEA) of the stave structure. This model assumes a heat transfer coefficient of $600W/m^2K$, as expected for the design flow, and an inlet fluid temperature of –15C. The maximum temperature on the structure is 2.4C on the hybrid, while the maximum temperature on the sensor is –3.9C. Experimental studies are underway to confirm the FEA results. Figure 60 shows the thermal distortions of the ladder. The out-of-plane distortion is expected to be below 10μ peak to peak. The longitudinal displacement corresponds to a net shrinkage of 15μ for the 300mm of stave modeled, or about 30μ for a full 600mm long stave.

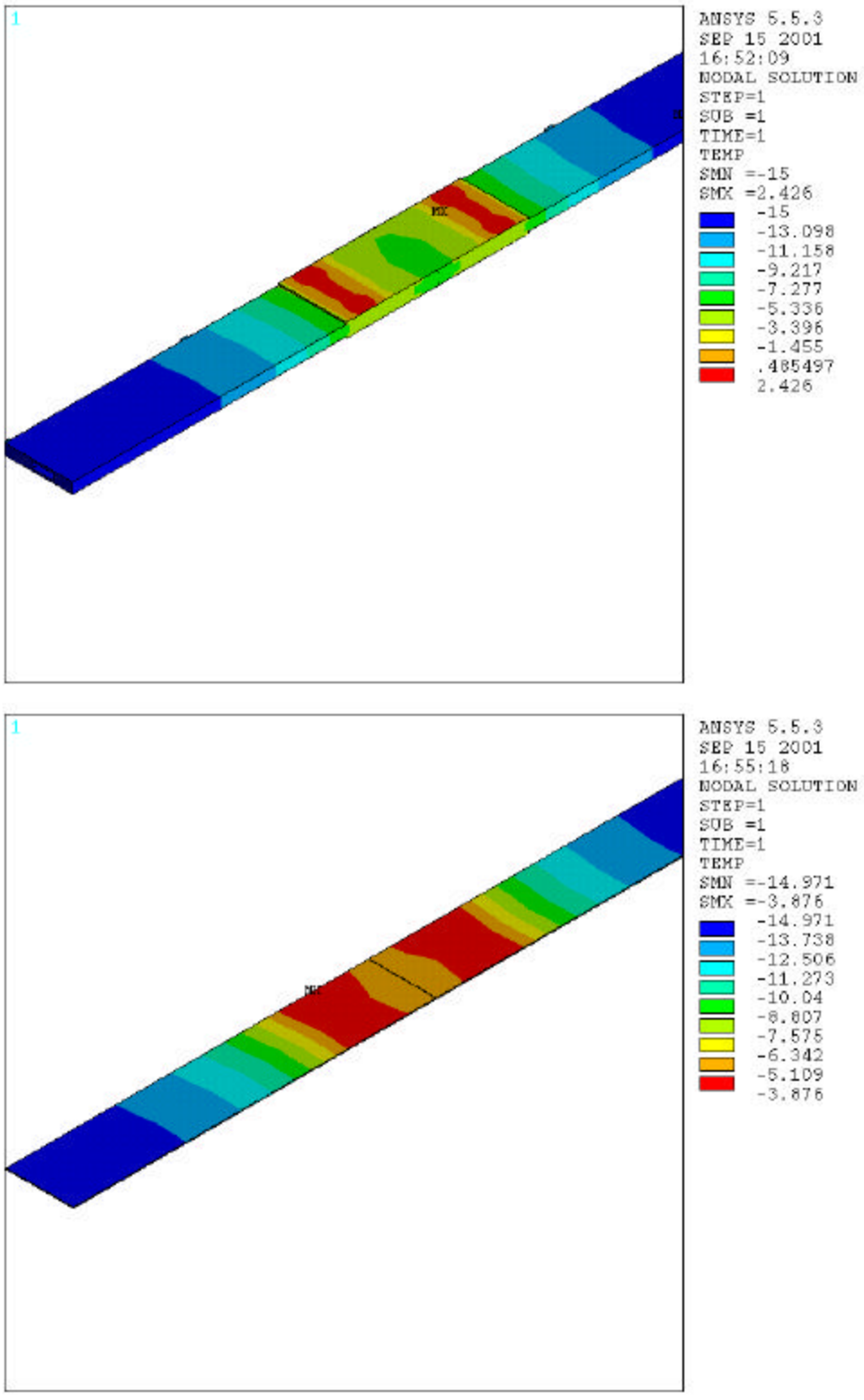


Figure 59: FEA results for the stave temperature profile. Coolant is assumed at -15C with a heat transfer coefficient of 600 W/m^2K. The upper plot shows the full stave structure, with the hottest region on the SVX chips, while the lower plot shows only the silicon sensor temperature profile.

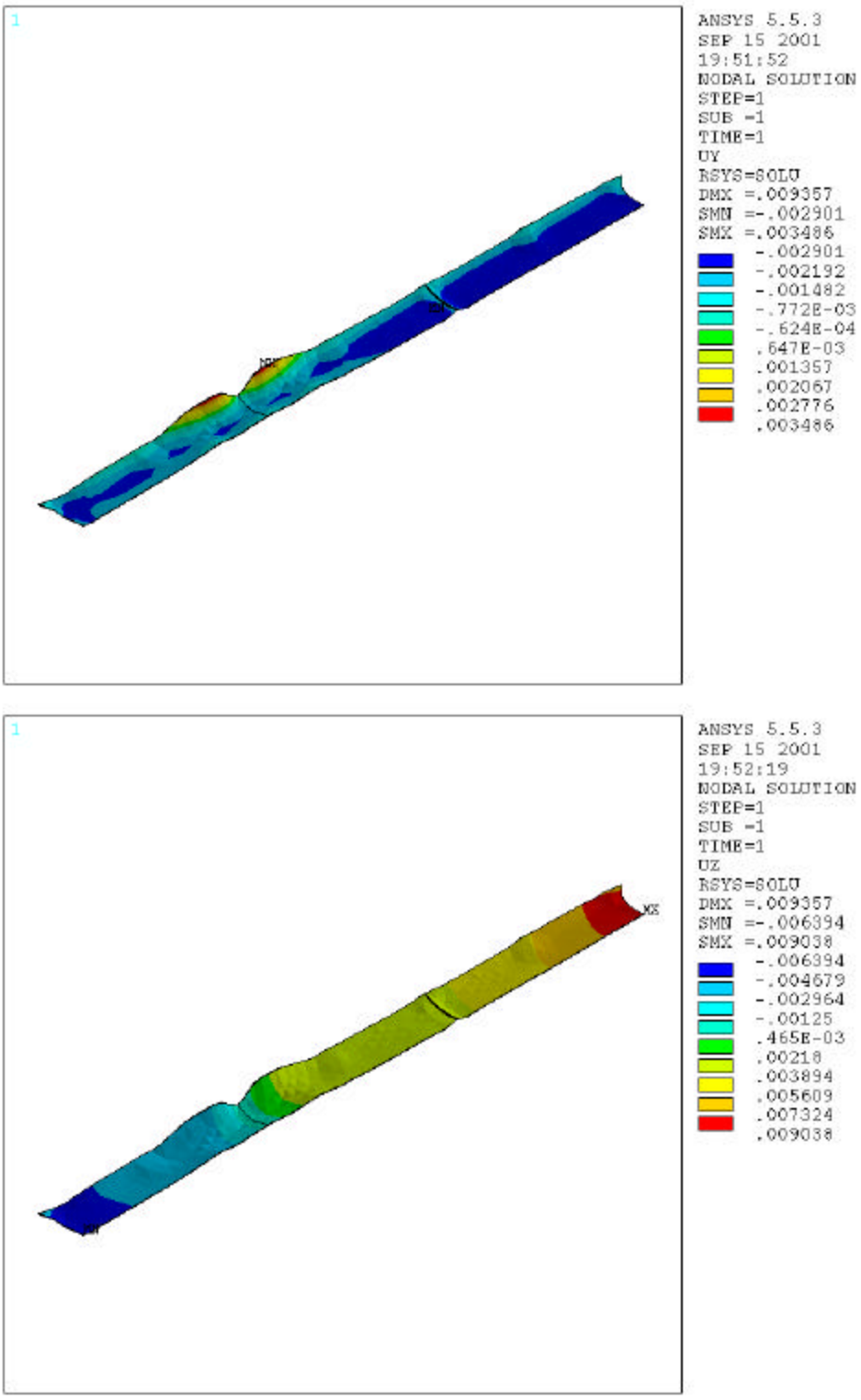


Figure 60: FEA results for the stave thermal distortion. Coolant temperature is –15C. Dimensions shown are in mm. The upper plot shows the displacement perpendicular to the sensor planes, the lower plot the displacement along the axis of the stave. Note that the model has only 300mm of the stave length and that the object shown is ½ width, where a symmetry boundary condition is used along the centerline (far edge) of the stave.

5.4.8 Layer 2-5 stave mechanical performance

Mechanical performance of the stave has been evaluated using both analytical and FEA calculations, with good agreement between these results. The expected deflection of the staves is less than 50-60μ with static gravitational loading (Figure 61). While somewhat larger deflections may not adversely affect the detector resolution, they lead to stave natural frequencies that are approaching the 60Hz range and the possible reduction in stave mass is negligible compared to the mass of the sensors, electronics and cables. In addition, reduced deflection allows for tighter installation and assembly clearances and easier handling during fabrication and installation of the staves into the barrel assemblies.

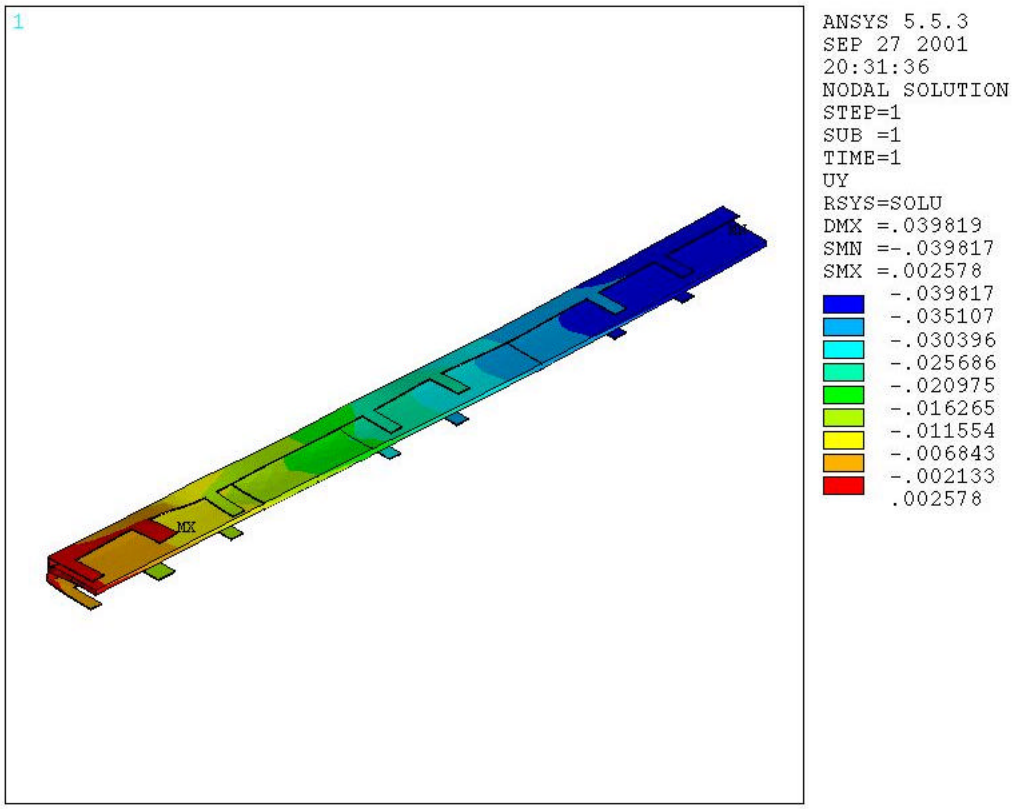


Figure 61: Stave deflection results for gravitational loading.

We have looked at extreme load conditions, for example application of a 1 kg load at the center of the stave, to study the robustness of the design. We find that, while the deflections are quite large, the stress levels in the sensors and structural elements remain far from failure levels. These studies were primarily aimed at understanding the handling requirements during fabrication and assembly.

A critical issue for the sensor alignment precision is deflection of the staves from external loads, in particular loads induced through the cables and cooling lines. To induce a 100μ deflection at the center of the beam requires a moment of 35kg-mm (3.0in-lbs). This is well above what could be induced through the external connections to the staves.

5.5 Installation Of The Run 2B Silicon Tracker

The Run 2B silicon tracker is to be delivered to the DØ experimental hall in two halves, north and south. We intend to deliver these halves in a manner similar to the one used for the Run 2A tracker. Unlike Run 2A, the two halves of the detector will be mated prior to installation into the central fiber tracker (CFT). This is necessary in order to achieve the required alignment. For Run 2A the two silicon barrel support structures were surveyed in the CFT on a CMM prior to installation of the CFT. The silicon was then aligned to the barrel support structures based on those surveys. This is not possible for the Run 2B device.

For Run 2A, each half of the detector was packaged in a protective enclosure prior to transportation. This enclosure provided mechanical protection of the assembly, storage for the cables attached to the assembly and a sealed gas volume that could be purged with nitrogen to prevent condensation and or contamination. The shipping enclosure also had an integrated rail system that was previously aligned to existing rails inside the CFT so that the detector halves could be slid directly into the CFT from the enclosure, one from each end. A set of roller bearings mounted from the enclosure provided a coupling to a trolley system used to move the silicon tracker inside the DØ detector cathedral and calorimeter gap areas. To reduce loads during transportation an air-ride cart was built which provided a stable rolling platform for each detector half. Once mounted inside the protective enclosure, each half of the detector was moved onto the cart. The cart was rolled to a loading bay, onto a truck lift gate and into the back of the truck. During several test runs and the final detector deliveries for Run 2A this cart consistently kept accelerations below 5g in all three directions. At DØ the cart was rolled back onto the lift gate and the detector was lifted off of the cart and delivered by crane to the assembly hall. At this point the detector was supported from above on roller bearings on a tube. This tube formed the first section of a trolley rail system used to bring the detector along the cathedral area into the calorimeter gap. When the detector arrived at the final turn into the CFT it was lowered onto a "table" mounted to the central calorimeter. Final alignment to the CFT was done by sliding the silicon tracker and enclosure base on the table surface.

For Run 2B we expect to use a similar enclosure for mechanical protection and dry gas purge. We will either reuse the existing air-ride cart or fabricate a similar one, for transporting the detector halves from the silicon detector facility to the DØ experimental hall. The detector is expected to remain on the beam line so it will not be possible to deliver the silicon tracker by crane directly from the truck to the detector cathedral area. Instead, the crane would be used to deliver the detector and cart to the floor of the assembly hall and the cart would then be rolled into the collision hall. A hoist would then be used to raise the silicon tracker up to the platform level. It may be possible to extend the trolley system used for the Run 2A installation to receive the Run 2B device directly from this hoist and deliver it to the calorimeter gap area. Both halves will be delivered to the same end of the CFT, mated and then slid into the CFT as one unit.

5.6 Alignment Within The Fiber Tracker

The Trigger Level II silicon track trigger (L2STT) [Ref DØ Note 3516, Sept 22, 1998] of the DØ detector imposes limitations on the permissible magnitude of coherent misalignment of the Silicon Detector. The L2STT allows the selection of events that contain decays of long-lived particles by performing a precise reconstruction of charged particle tracks in the Silicon Detector and the CFT.

In addition to improving the resolution of the measurement of track p_T over that of the CFT alone (by a factor of 2-3 depending on p_T), the L2STT also determines the impact parameter of charged tracks with respect to the nominal beam position. If the beam is tilted, or offset laterally, with respect to the Silicon Detector, tracks with large fake impact parameters becomes excessive, giving rise to unwanted triggers. Monte-Carlo study of ttbar and B events has shown that it is necessary to limit angular misalignment of the Silicon Detector with respect to the beam to less than ±200 μrad to limit the fraction of fakes to less than 5% for impact parameters of 100μ.

Lateral offsets should be kept below 1 mm to limit inefficiencies due to tracks crossing Silicon sectors. Lateral offsets of less than 1 mm are expected to be achievable by final realignment of the detector , and it is expected that orbit tuning can reduce residual lateral offsets to nominally zero after they are measured by the Silicon Detector.

The same angular constraints apply to the beam during stores, and the lateral position of the beam must be held steady to 30μ or so to avoid creation of an increased trigger rate due to apparent impact parameter increase. During Run I, CDF showed that lateral variations during stores did not typically exceed 40μ and angular variations were typically too small to measure. Angular variations store-to-store varied less than 100μrad. DØ has not yet measured these quantities to this precision in Run 2, but expects to completely characterize the behavior of the beam as Run 2A continues and the DØ geometrical reconstruction matures.

The present Run 2A Silicon Detector has already been shown to be aligned to the CFT to ± 70 μ at any individual silicon sensor. Since the overall length of the sensor staves of the Run 2B Silicon Detector is on the order of 1 m, such potential misalignment leads to well below 100 μrad of angular misalignment of the stave. It is intended to "recycle" the present mounting system between the CFT and the Run 2A Silicon Detector in such a manner that the quality of this relative alignment is not lost.

For this reason, and in view of the constraints on the required alignment, no type of dynamic alignment mechanism is contemplated for the Run 2B Silicon Detector. Precision fiducials will be provided on the silicon detector to enable the installed position of the device to be related to that of the existing CFT, so that the precision of this relationship can be verified after installation is completed.

5.7 Mechanical Infrastructure At DAB

5.7.1 Cooling system

DØ installed the two-piece Silicon Detector for Run 2A into the DØ fiber tracker in late 2000 and early 2001. Those two pieces are referred to the South half and the North half. Each half is read out by onboard electronics that generates heat which must be removed. Removal of that heat is performed by redundant chillers that circulate a glycol and water mixture in parallel closed loop systems with a common coolant reservoir. The coolant of the existing system is chilled to –10° C. For Run 2B, an additional system will be added to chill a portion of the coolant to -20° C.

Silicon in Layers 0-1 will be cooled to -10^{o} C while Layers 2-5 will be cooled to a minimum temperature of -5^{o} C. A temperature gradient may be allowed in Layers 2-5, with -5^{o} C at Layer 2 and a maximum temperature of $+5^{o}$ C at Layer 5. These temperatures will be achieved using a water-glycol cooling loop.

Use of the existing cooling system in place for Run 2A is possible, but with modifications to provide the two-tiered cooling needs of Run 2B. Currently the cooling system circulates 30% by volume ethylene glycol at -10^{o} C to the detector. For Run 2B, one glycol stream will need to be chilled to -20^{o} C for Layers 0 and 1 while a second stream will need to be -15^{o} C for outer Layers 2-5. Much of the existing piping and process control system can be preserved if a second chiller and supply line is provided for the colder silicon layers while allowing both streams to use the existing return lines in common. The existing chiller has a cooling specification of 4400 W at -10^{o} C and was tested to deliver 5500 W during actual tests at Fermilab.

To prevent freeze-out of coolant in the chillers, the freezing point of the circulating mixture must be 5.9^{o} C lower (10 F) than the fluid's control point temperature. Since coolant will be chilled to -20^{o} C, the fluid's freezing point must be -25.6^{o} C or lower. A glycol concentration of 41% by volume is chosen for the system, which has a freezing point of -25.9^{o} C. A 41% ethylene glycol, 59% water mixture by volume has the following properties which are used to define the Run 2B detector's flow rate and pressure drop limits if the existing system is to be used: at -20^{o} C, density = 1073.5 kg/m^3, viscosity = .01638 N/(m^2-s), vapor pressure = 0.7 mmHg.

To avoid risk of pump cavitation, the minimum allowable pump suction pressure is –10.4 PSIG. The calculation assumes a required pump NPSH = 8 FT and that the fluid vapor pressure is high (pv = 18.1 mmHg) at startup because the fluid is warm. The pump suction pressure is determined by system flow losses (the pressure drops both in the piping and the detector) and the elevation of the detector relative to the pump. The detector is about 3.96 meters above the pump intake. Piping flow losses are calculated using an Excel spreadsheet developed by Herman Cease for Run 2A but using fluid properties of 41% glycol, 59% water mixture at -20^{o} C. Table 6 (below) summarizes calculations by providing maximum pressure drops allowed across the detector for two possible flow rates, 10 GPM and 12 GPM.

Table 6 - Maximum Allowable Pressure Drop Across Detector

Coolant flow rate	**10 GPM**	**12 GPM**
P_s, minimum pump suction pressure to avoid cavitation	-10.4 PSI	-10.4 PSI
-(Head), due to detector elevation = 3.96 m	-6.1 PSI	-6.1 PSI
$-dP_{pipes}$, piping flow losses	6.1 PSI	8.3 PSI
Max allowable flow losses across detector, $\mathbf{dP_{det} = P_s - Head - dP_{pipes}}$	**-10.4 PSI**	**-8.2 PSI**

The table shows the tradeoff to be considered to cool the detector. If higher flow rates are desired, the flow passages must be far less restrictive to limit pressure drops. The calculations above are concerned only with piping downstream of the system's expansion tank, since only those components control the suction pressure at the pump. Flow losses in the piping are calculated for existing piping only. As discussed above, a new separate supply line is required to deliver -20^o C fluid to the inner layers, while the existing piping would supply fluid to Layers 2-5. The calculations therefore assume that the new parallel stream supplying coolant to the inner layers will have losses equivalent the existing piping supplying Layers 2-5.

5.7.2 Dry gas system

Temperatures inside the detector will be as much as 30^o C cooler than the maximum ambient dew point temperature (typically 10^o C) maintained by D-Zero's HVAC system. It is critical that moist ambient air be displaced from the detector volume with a dry purge source to prevent the formation of condensate and ice.

The existing dry gas purge and process control systems will be used for Run 2B, but the compressors, dryers, and cooling system will require appropriate maintenance after five years of continued service. The dry gas source proved failsafe for Run 2A through a 'What-If' failure analysis. An additional 'What-If' analysis is required if any changes are made for Run 2B. The dry gas system remains operational during all probable failure modes or has enough of a dry gas reservoir to continue to purge the detector until it is warmed above building dew point temperature. The purge source is reliable through extreme summer (40^o C, 100% relative humidity) and winter (-35 C) weather. The system is capable of delivering 60 SCFM of dry air purge. The maximum dew point temperature of the delivered gas is -60^o C.

5.7.3 Monitoring, interlocks, and controls

Monitoring, control, and interlock functions for the dry purge system and the silicon cooling system were added to the existing system commonly known as the DØ Cryo Control System for monitoring, interlocks, and alarming.

Mechanical piping and vessels of the dry gas and cooling systems were designed and fabricated with proper safety and relief devices so that the monitoring and interlock systems are not relied upon for personnel safety. All electrical loads have proper overload protection.

The Silicon Detector power system has an extensive *internal* interlock protection scheme provided by its power supply and processor control and data acquisition electronics

Thirty RTD temperature sensors were installed throughout the VLPC fiber barrel structure in order to track the fiber barrel temperatures as the Silicon system is cooled and its purge air flows are adjusted. Those thirty temperature sensors are displayed on the silicon computer graphics pictures.

5.7.4 Systems electrical power

DØ has backup electrical power provided by a diesel generator that starts automatically upon commercial power loss. The Silicon purge air compressors, the Silicon chiller cabinets, and the U.P.S. that supplies power to the Silicon cooling system control system are all on backup power. The silicon cooling system monitoring and interlock systems are powered by a U.P.S., which prevents power interruption to those control systems.

5.7.5 Existing chiller overview

There are two chiller cabinets, they have been designated chiller #1 and chiller #2. They are commercial units which contain a coolant pump, a chiller compressor, and the associated motor controls to run and control the unit. The temperature control is a stand alone single loop controller with a relay output and it is mounted on the chiller cabinet.

The chiller cabinet motor controls have been modified for remote interlock control. The remote interlocks have been implemented using solid state relays. See attached electrical drawing for details.

Each chiller has two bypass key-switches built into the cabinet. One key switch overrides the external pump interlocks while the other key switch overrides the external cooling interlocks. These were installed for emergency and diagnostic reasons. The keys to these key-switches will be administratively controlled.

5.7.6 Additional chiller overview

Two chiller cabinets will be added for the additional cooling loop expected to operate at -20° C. They have been designated chiller #3 and chiller #4. Either can be the active chiller with the

other as a backup but not running. These will be have interlocks and key switches similar to the original chillers.

5.7.7 Current process control system overview

The current process control system is based on a number of commercial Siemens Programmable Logic Controllers (PLC's) and is commonly referred to as the CRYO control system. These PLC's are capable of handling thousands of physical I/O through remote I/O bases. These remote I/O bases can have many types of modules installed in any of the slots for handling different types of field I/O. These PLC's are commercial computers which have many prewritten communication drivers available. Programming the PLC's is also done through commercial software.

The operator interface is based on the commercial distributed control platform of Intellutions FIX32. FIX32 provides computer alarms, graphical pictures with real time values, operator security, and historical collection of data. The use of FIX32 originated at DØ and is now commonly used throughout the Lab.

The Cryo Control System monitors and controls the Helium Refrigerator, LAR Calorimeters Cryo, Super conducting Solenoid cryo, Instrument Air, Vacuum, Building HVAC, WAMUS and Solenoid magnet power supplies, and the VLPC cryo.

5.7.8 Silicon cooling system integration into the current process control system

The Cryo control system was expanded with the addition of I/O base eleven on the South sidewalk and I/O bases seven, eight, and ten on the detector platform in order to pickup the physical field devices for the Silicon cooling system and dry purge air system.

The Silicon cooling system and dry purge air system logic programming were added to the PLC which has plenty of program capacity.

The Silicon cooling system and dry purge air system computer graphical pictures and database blocks were developed and added to the FIX32 system.

5.7.9 Silicon cooling system computer security

The Silicon Cooling System's computer security, along with all of DØ's other process control system's computer security are provided by a combination of Intellution's FIX32 and Microsoft's NT Operating System Platform.

The computer system's infrastructure is controlled and protected by Microsoft's Windows NT Domain Controllers. This infrastructure includes domain user accounts, server file protection, Remote Access Services (RAS), and distributed networking. This is the "DMACS" domain at Fermilab. There are currently three domain controllers, two at DØ and one at CDF. This domain is shared by many groups at Fermilab. The domain administrators control the domains user accounts and file privileges.

The process control system's security is provided by Intellutions's Fix32 and Fix Dynamics. This security is setup by the system developers who draw the pictures and build the databases. The system developers lay out their system based on a predefined set of rules. They then grant privileges to the users and operators who would need some control over these systems. These "privileges" are what allows some and denies others access to opening and closing a valve for instance.

Remote Process Control System access is provided by an NT RAS connection and Microsoft's NetMeeting. Remote access allows someone to view process data from home or elsewhere. The NT RAS security is provided by the NT domain controller, this security is essentially someone logging into the domain through a modem connection. NetMeeting allows someone to remotely take control of a workstations desktop. NetMeeting only allows an administrator to do this. The Process Control System security through NetMeeting is handled by NetMeeting, FIX32 or Dynamics, and the NT domain controllers. Other future remote access paths include the Internet i.e. a WebSite, however this is not well developed at this time.

5.7.10 Monitoring via the DAQ system

The DØ physics data acquisition and file system commonly referred to as the DZERO DAQ system will have access to the Silicon data along with all the other process control data. All the process data will be stored on a SCADA node dedicated to accessing and conditioning data just for the DAQ system. The DAQ programmers will be responsible for organizing a data polling list, then manipulating and storing the data in the physics file system. They may also choose to setup some sort of alarm system.

5.7.11 Interlocks

All interlock design and wiring practices use "failsafe" methods. That is a device must have positive feedback to its electronic circuits or it is considered "tripped". For example, a normally closed contact would be used on temperature switch in the field. This allows for a lost signal or a disconnected field device to generate a tripped condition. Discriminator modules are used in this system in order to convert an analog value into a discrete signal. These modules are all configured in their failsafe mode, which allows for loss of signal or transmitter failure to result in a tripped condition.

There is one exception to the failsafe practice in the Silicon Cooling System design. That is the control of the cooling circuit in the chiller cabinets. The chiller cooling control is called the Hot Bypass valve, when this valve is energized the chiller is not cooling. If the control signal is lost, the chiller would be forced into the cooling mode, since a solid state relay is used to control this circuit. This scenario has been countered by using this same DC control voltage that controls the Hot Bypass control, to control the main chiller power solid state relay. Therefore, if the DC control voltage were lost for any reason the entire chiller would shutdown.

Interlock Layers

The Silicon detector has two functional interlock layers. The primary power interlock system is embedded in the detector power supply and its control system. This system is capable of

monitoring temperature and other parameters and shutting down individual channels and groups of channels.

The secondary interlock system is based around the cooling system parameters and referred to as the external interlock system. The external interlock system is designed to protect the Silicon detector from temperature and dew point limits.

5.7.12 Alarms

The Silicon cooling system may run attended or unattended by operators. The alarms have been picked, programmed, and configured to be consistent with the other systems that the control system runs and monitors.

Alarm Layers

DØ incorporates a layered alarm strategy. There are typically three layers of alarms. The first is a computer alarm that notes when a parameter is slightly out of normal tolerance. The second is a computer alarm when a parameters is more than slightly out of tolerance. The third is an Auto-Dialer alarm when the parameter is at a point where immediate attention is necessary.

Computer Alarms

Computer alarms are generated by the FIX32 software mentioned earlier in this paper. An operator with the correct security privileges may set the alarm thresholds and also acknowledge these alarms.

A computer alarm can be routed and filtered by any of many FIX32 nodes throughout DØ and Fermilab. When a computer alarm occurs, all the FIX32 nodes that are set up to filter in the alarm area of a particular alarm will start beeping. This beeping will continue until the alarm condition is cleared and the alarm is acknowledged.

AutoDialer Alarms

An operator with the correct security privileges may set the alarm thresholds and also acknowledge these alarms.

The Auto-Dialer alarm is generated by the PLC and a computer dedicated to running a software package called WIN911. This software package is capable of paging people's pagers with a numeric code as well as calling inside and outside the lab using the telephone system with a voice synthesized message. The Auto-Dialer is preprogrammed with a list of "experts" who can deal with the particular systems' problem that created the alarm. The Auto-Dialer will continue paging and calling people serially on this list until someone acknowledges the alarm or the alarm condition ceases.

The Auto-Dialer is what really makes unattended operation practical at DØ.

DAQ Alarms

All the PLC data from all process systems will be available to the programmers that program the DØ DAQ system. Once this data is picked sorted the programmers will likely set up a set of alarms. This assumption is based on last run's experience. The infrastructure for this data transfer is well defined and in progress of being implemented. The data sets remain to be defined.

CHAPTER 6 - READOUT ELECTRONICS

6.1 Overview

The readout system for the Run 2B silicon detector will be based on the new SVX4 chip and the existing Run 2A silicon data acquisition system. Sensors are connected to the outside world through hybrids with the SVX4 chips, and an external path consisting in turn of low mass jumper cables, junction cards, twisted-pair cables, adapter cards, and high mass cables followed by Interface Boards, Sequencers and VME Readout Buffers. A brief overview of the main ingredients of the readout system is presented in this section. Conservative solutions allowing for the fastest implementation of necessary changes were favored among different design options.

The SVX4 chip, designed as a joint DØ & CDF project, will be able to function in SVX2 mode and, therefore, will be compatible with the Run 2A readout electronics as discussed in detail in the next section. The chips will be mounted on hybrids. In the outer layers, the hybrids will be glued directly onto the silicon sensors. This allows for wire bonding directly from the chips to the sensors. The readout concept for staves in Layers 1 through 5 is shown in Figure 62. A "double-ended" hybrid design is chosen where chips are mounted on both ends of the hybrid and bonded to two different sensors. The hybrids are fabricated using thick-film technology on a beryllia ceramic substrate. All SVX4 chips on the hybrid are daisy chained for readout through one low mass digital Jumper Cable to the Junction Card. In Layers 2, 3, 4 and 5, the hybrid has 10 SVX4 chips and there are four readout cables per stave: two for axial sensors and two for stereo sensors. In Layer 1, 6-chip hybrids are used and there are three readout cables per phi segment.

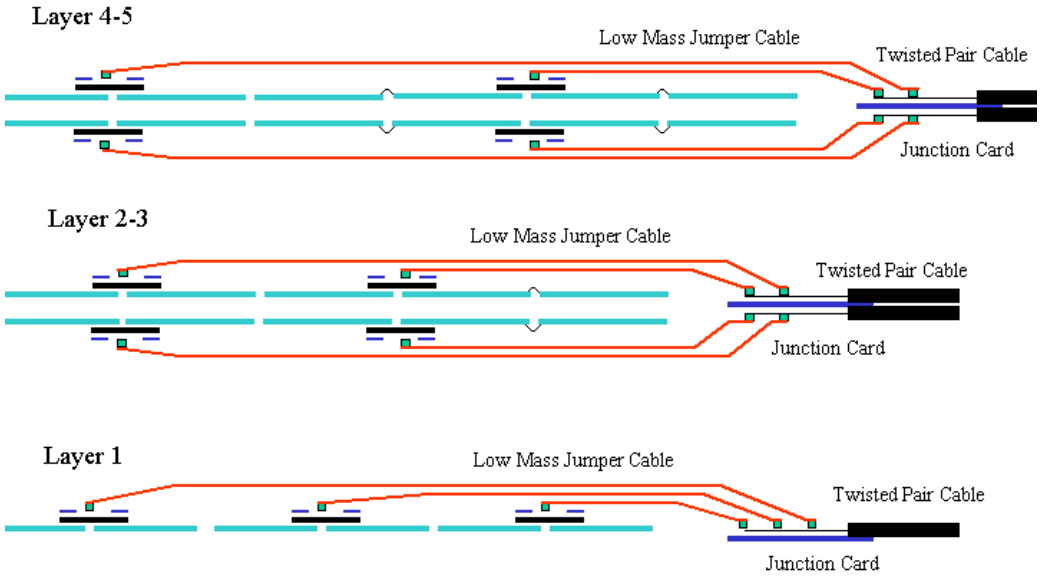


Figure 62 - Concept of readout for Layers 1 through 5

The innermost layer requires a substantially different design due to its very small radius and stringent requirements on the amount of material. For this layer, low mass analog readout cables

will couple the silicon and hybrids as shown in Figure 63. This allows the hybrids and silicon to be mounted independently, moving the mass and heat load of the hybrids out of the active detector volume. One 2-chip hybrid reads out one silicon sensor. To equalize the length of the analog cable between different sensors, the sensor closest to z=0 is connected to the closest hybrid. Digital jumper cables connect the hybrids to Junction Cards. While the added capacitance from the flex cable degrades the signal-to-noise (S/N) ratio, we expect to achieve a S/N>10 for the SVX4 with analog cable readout even at the end of Run 2B as was explained in Section 4.3. Section 6.3 discusses issues related to the analog cables.

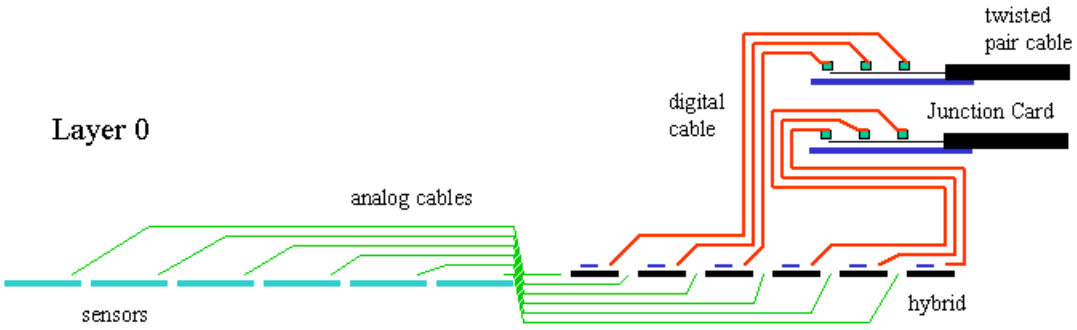


Figure 63 - Concept of readout for Layer 0

The total readout cable count is 888 with the cable count per layer given in Table 7. A detailed discussion of the hybrid and stave electrical properties is presented in Section 6.4.

Table 7 - Cable count per Layer

Layer	***Chips per hybrid***	***# readout cables***
0	2	144
1	6	72
2	10	96
3	10	144
4	10	192
5	10	240

A major consideration in the design has been to preserve as much of the existing Run 2A silicon data acquisition system as possible and to reuse the associated cable plant. Nevertheless, a few modifications are necessary to address two important issues:

1. The SVX4, produced in 0.25 micron technology will require lower operational voltage, 2.5 V as compared to 5 V necessary for SVX2. The allowed operational range of 2.25 – 2.75 V for SVX4 poses significant restrictions on the voltage drop in the power lines.

2. Modification of control signals are needed to accommodate the difference between the SVX2 chip and the SVX4 chip operating in SVX2 mode.

Figure 64 shows a block diagram of the Run 2A silicon data acquisition. SVX2 chips are read out with approximately 2.5 meter long low mass cables to the passive Adapter Cards located on the face of the calorimeter (Horseshoe). Interface Boards are connected to the Adaptor Cards with 6 meter long 80 conductor cables and serve as distributors of low voltages, bias voltages, data and control sequences for the detector. Sequencers on the Platform provide clock and control signals for the SVX2 chips. The sequencers are also used to read out data from the chips and send them to the VME Readout Buffers via optical fibers. Only parts highlighted in gray will be modified for the Run 2B readout system. Adapter Cards and Low Mass Cables will be replaced with new components. Some firmware modifications in the sequencers will also be required as discussed in Section 6.11.

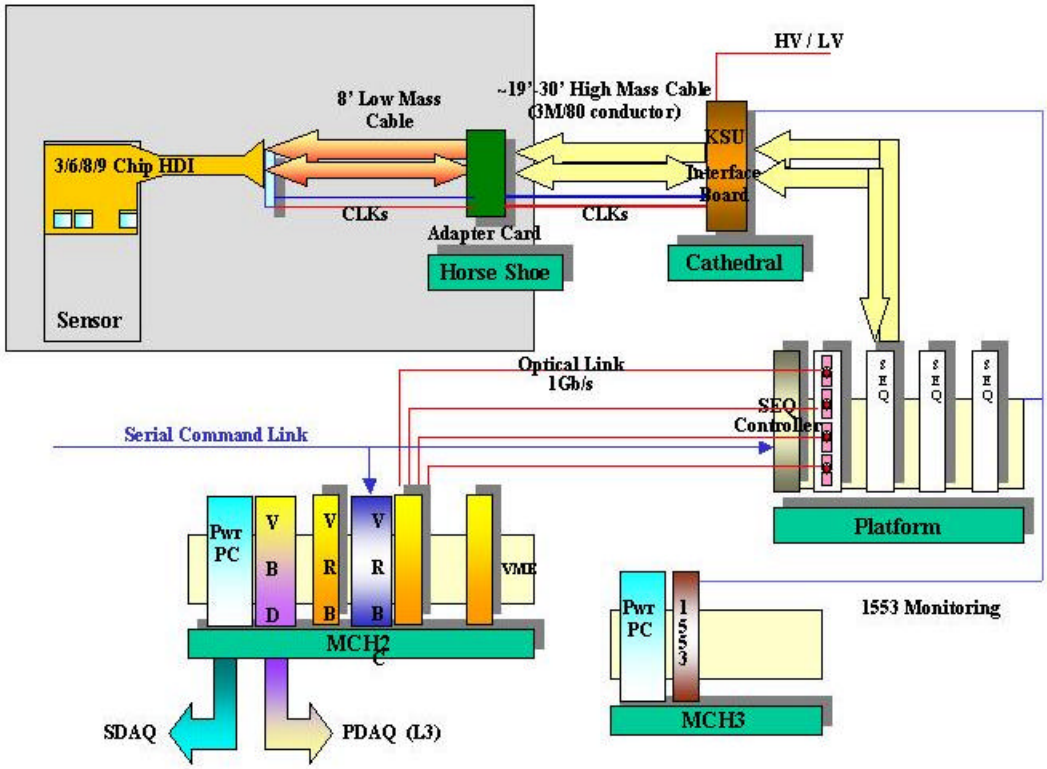


Figure 64 - Block diagram of the Run 2A silicon data acquisition system

Figure 65 shows the block diagram of the new components for the Run 2B data acquisition system. The Run 2A philosophy, having each hybrid connected to a single Interface Board channel, is preserved. The Interface Board provides all necessary voltages and communications to and from the hybrid. It also monitors the temperatures and low voltages. However, the

segmentation of this connection and the functionality of the intermediate pieces is different from that in Run 2A. A short low mass jumper cable starts from the hybrid and goes to the back of the detector where a passive junction card is located. The junction card is connected to a new Adapter Card via a 2.4 meter long twisted pair cable. Data lines are driven differentially from SVX4 chips to the Adapter Card in contrast to the Run 2A approach which has single ended readout. Downstream of the Adapter Card, the lines are single ended.

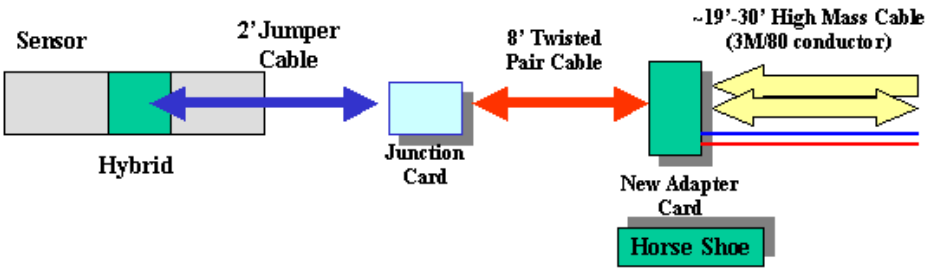


Figure 65 - Block diagram of the new components of the Run 2B data acquisition system

The Adapter Card is the key new component of the data acquisition accommodating most of the necessary changes. It will perform the voltage regulation and will contain simple logic for the SVX4/SVX2 conversion as explained in Section 6.9. The Adapter Card is connected to the Interface Board with the existing 80 conductor cable. Some changes required for the Interface Boards are described in Section 6.10. Sections 6.6, 6.7, and 6.8 contain information about low mass Jumper Cables, Junction Cards and Twisted Pair Cables. Sections 6.12 and 6.13 have a discussion about low voltage and high voltage supplies and distribution. Results of simulations related to the readout performance are presented in Section 6.14.

6.2 SVX4 Readout Chip

The readout of the detector is accomplished by the use of the SVX4 readout chip, which is presently under development. The SVX4 is the last of a series of chips developed for silicon sensor readout by the FNAL-LBL collaboration. Earlier versions of such chips were the SVX-B and SVX-H (used in the readout of the first silicon vertex detectors of CDF), the SVX-2 (used in the present DØ detector), and the SVX-3 (used in the present CDF vertex detector). The SVX4 design thus draws heavily upon the experience gained from these earlier efforts and incorporates many of the desired features gleaned from this experience.

The SVX4 is, like the SVX2 and SVX3, a chip with 128 inputs with a 48 micron pitch, which receive the charge generated by 128 strips of a silicon detector. The input charge, for a well-defined period of time corresponding to a single beam crossing, is integrated and deposited in a capacitor of a switch-capacitor array called the pipeline. This pipeline has 42 cells, thus allowing the successive storage of the charge generated during 42 successive beam crossings. If an event is accepted by the Level 1 trigger framework during any one of the 42 beam crossings, the charge of the appropriate capacitor is digitized by an on board ADC, and the resulting digitized

data is presented to the data acquisition system. The data can be read in a read-all mode (i.e. in its totality), in a zero-suppressed mode (i.e. only channels above a certain threshold value), or in a zero-suppressed mode with neighbors (i.e. in addition to the channels above threshold the channels flanking them are also read out). The chip also has a dead-timeless feature, which allows for the concurrent acquisition of charge by the integrators and the pipeline while digitization is also taking place; this feature – which is the salient difference between SVX2 and SVX4 - will not be used by DØ.

The SVX4 will be produced in a deep submicron process (0.25 micron) by TSMC (Taiwan Semiconductor Manufacturing Corporation). Such submicron processing leads to a very small oxide layer which in turn leads to a highly radiation tolerant device, without having to resort to any special manufacturing processing. Chips developed in such process (such as the APV25 chip for the CMS experiment and the VA1 chip for the Belle experiment) have been subjected to radiation doses exceeding 20Mrad with no sign of radiation damage, and will survive the expected doses for all layers of our detector. These submicron process chips require a power supply of +2.5 V, which is different from the +5V and +3.5V of the existing SVX2.

The SVX4 chip, to the extent feasible, is a copy of the SVX3 chip used in the present CDF detector. As such it incorporates features that were not used in the SVX2 and are not part of the control and readout configuration of the Run 2A silicon data acquisition system. These features have to do mostly with the deadtimeless operation mode of the SVX3 and consist mostly of the presence of additional control lines and of a dual clock (front- and back-end clocks). The question was raised late last year if the SVX4 could be used with the DØ readout system and what modifications would be required. As it turned out a simple scheme that remapped our control lines to the ones required for the SVX3, which channeled our clock to either the front-end or the back-end clock depending on the mode of operation of the chip, turned out to be adequate. A test board consisting of a single FPGA and simple transceivers was able to perform the required task, and an SVX3 chip was read by the DØ sequencer board, as seen in Figure 66.

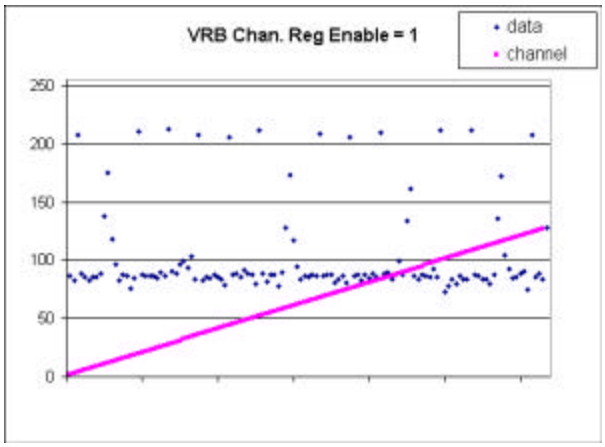


Figure 66 - SVX3 chip performing in SVX2 mode with the DØ data acquisition system (November 2000)

As a result of this successful demonstration, DØ adopted the SVX4 chip being designed by a FNAL-LBL-Padova team of engineers and has played an active and significant role in the design

effort. A single common chip that will satisfy the needs of both CDF and DØ will be used. The remapping shown in Table 8 can be accommodated by the existing DØ Sequencer readout module. In addition, the use of internal circuitry of the SVX4 allows the chip to operate in the so-called DØ mode. The circuitry can be turned off via an external wirebond to the digital voltage line for operation in the CDF mode. In the DØ mode, using internal gating, the clock is sent to the appropriate section (front/back end) depending on the chip's internal mode. The same selector also forces the chip to use the PRD1, PRD2, L1A, and CALSR as inputs from the bi-directional differential data bus (for DØ) rather than their single ended dedicated input pads (for CDF). Thus, to be able to use the existing DØ readout sequencers the only major change required is a new adapter card with transceivers that will adapt the single-ended, 5V signals used by the sequencer to differential, 2.5V signals used by the SVX4.

The design of the chip is proceeding at a good pace. Prototype chips have been fabricated; these chips included only the preamplifier and the capacitor pipeline. A preamplifier design with excellent frequency response, good reset time, good power supply noise rejection, and good noise performance has been identified. The overall noise of the analog section (i.e. preamp and pipeline combined) has been measured as 450e+43e/pF, where the last term shows the noise dependence on the input load capacitance. The measurement has been performed with 100 nsec sampling time and 70 nsec preamplifier rise time. These parameters are close to optimum for 132 nsec operation. Irradiation of the test chip to 16 Mrad with a ^{60}Co gamma ray source did not show any significant performance degradation.

The digital end of the chip (back end) remains to be completed. It is anticipated that the first fabrication run of complete chips (for engineering and evaluation purposes) will take place in late 2001, and prototype chips will be available just before the end of 2001. We are in the process of setting up test rigs to evaluate these chips, and we are in the process of designing test boards and developing test software and procedures.

Table 8 - Mapping between SVX2 and SVX4 readout/control lines

SVX II				***SVX4***			
Mode				Mode			
INIT	ACQ	DIG	READ	INIT	ACQ	DIG	READ
BUS 0 PA RESET	BUS 0 PA RESET	BUS 0 PA RESET	Data 0	BUS4 PARST	BUS4 PARST	BUS4 PARST	Data4
BUS1 RREF-SEL	NC	HIGH	Data 1	BUS3 RREF-SEL	BUS3 RREF-SEL	BUS3 RREF-SEL	Data3
BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	BUS2 PIPE-ACQ	Data2	BUS5 L1A	BUS5 L1A	BUS5 L1A	Data5
BUS 3 PIPE SREF	BUS 3 PIPE SREF	BUS 3 PIPE SREF	Data 3	BUS 6 PRD1	BUS 6 PRD1	BUS 6 PRD1	Data 6
BUS4 CNTR RESET	BUS4 CNTR RESET	BUS4 CNTR RESET	Data4	BUS2 PRD2	BUS2 PRD2	BUS2 PRD2	Data2
BUS5 RAMP RESET	BUS5 RAMP RESET	BUS5 RAMP RESET	Data5	BUS 1 RAMP RESET	BUS 1 RAMP RESET	BUS 1 RAMP RESET	Data1
BUS6 COMP RESET	BUS6 COMP RESET	BUS6 COMP RESET	Data6	BUS0 COMP RESET	BUS0 COMP RESET	BUS0 COMP RESET	Data0
BUS7 SR LOAD	BUS7 CAL INJECT	BUS7 N/C	Data7	BUS 7 CAL/SR	BUS 7 CAL/SR	BUS 7	Data7
MODE0	MODE0	MODE0	MODE0	FEMOD	FEMOD	FEMOD	FEMOD
MODE1	MODE1	MODE1	MODE1	BEMOD	BEMOD	BEMOD	BEMOD
CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE	CHNG MODE
TN	TN	TN	TN	TN	TN	TN	TN
BN	BN	BN	BN	BN	BN	BN	BN
CLK	CLK	CLK	CLK	FECLK	FECLK	BECLK	BECLK
CLKB	CLKB	CLKB	CLKB	FECLKBAR	FECLKBAR	BECLKBAR	BECLKBAR
DATA VALID	DATA VALID	DATA VALID	DATA VALID	OBDV	OBDV	OBDV	OBDV
PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN	PRIORITY IN
PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT	PRIORITY OUT

6.3 Analog Cables

In the current design of Layer 0, the analog signals from the silicon sensors are transmitted to the hybrid with the SVX4 chips by flexible circuits with fine pitch copper traces, up to 500 mm long. While very attractive because of material and heat removal from the sensitive volume, this approach represents a considerable technical challenge. The addition of the analog cable deteriorates the noise performance of the silicon sensors. Procurement of the flex cables and the complicated ladder assembly are other non-trivial issues. Nevertheless, a similar design is used by CDF for the readout of the innermost layer L00 in Run2A, which can be considered as a proof of technical feasibility.

One of the most important aspects in the design and technical realization of a long analog cable is the capacitance between the traces, which has to be as small as possible. Any load capacitance will contribute to the noise seen by the preamplifier. Fanning out the cable traces from the nominal pitch of 50 micron to a larger pitch, for example 100 micron, after the first few centimeters, can reduce the capacitance of the cable. Analytical calculations show that the capacitance per unit length can then be smaller by 30-40% if the trace width is kept constant, as shown in Figure 67.

The flexible dielectric substrate of the cable also affects the capacitance. The material of choice in high energy applications is polyimide, like Kapton HN with a dielectric constant of 3.5 at a frequency of 1MHz. This material is radiation hard with good mechanical and electrical properties. Other synthesized polyimide materials on the market achieve a lower dielectric constant by adding halogens. They are not radiation hard and are not in compliance with CERN and Fermilab fire safety regulations. Materials like polyethylene or polypropylenes, although used in the flex industry and possessing a lower dielectric constant are also not radiation hard up to the 10-15 Mrad level, to which the innermost layer of the silicon tracker will be exposed. The material choices for the flex cable are, therefore, limited to the standard polyimide.

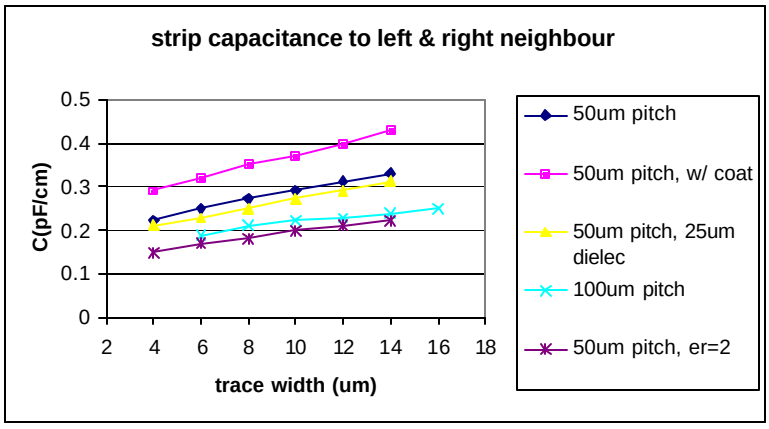


Figure 67 - Analytical calculations of the capacitance per unit length as function of the trace width. The capacitance is defined as the capacitance of one trace to the left and right neighbor trace. The beneficial effect of going to lower trace widths and larger pitch is shown.

A 500 mm long Kapton based flex circuit cable with a small pitch of only 50 micron represents a major challenge for flex circuit manufacturers. The printed circuit workshop at CERN that produced such cables for CDF in 1999 has been reorganized focusing on circuits for the LHC experiments and, most likely, will not be available for the Run 2B production.

Since the manufacturing challenge of such long fine pitch cables was recognized early, DØ has started working with potential vendors. Based on good prior experience with high density interconnects (HDI) from Dyconex Inc. in Zurich, Switzerland, we contacted them in May 2001. At that time Dyconex was in the process of commissioning a new thermal direct imaging (TDI) system for very fine line and space patterning for PCBs and HDIs. The new technology exploits an IR laser system and an infrared sensitive, thermally activated, liquid photoresist for high accuracy imaging and registration.

DØ placed an order for an engineering sample with Dyconex in June 2001 with a goal to reproduce the CDF analog cable and qualify Dyconex as a possible vendor. Dyconex will use the TDI method to fabricate our circuit sample. As of this date they have collected enough experience in test runs and are convinced that the TDI is the appropriate technology choice for this task. The first TDI results are encouraging. They could achieve an image transfer of the CDF cable layout via TDI with good reproducibility. However, the optimal material for the dielectric polyimide substrate was not yet found, since several polyimide foils with adhesiveless copper cladding showed signs of delamination after thermal imaging. A 50 micron thick polyimide foil with a cast copper layer performed best so far and better material with stronger copper adhesion has been ordered.

Dyconex is planning to achieve ultra fine copper lines with 5 micron trace width which is at the technological edge of the TDI method. They are aiming for 6-7 micron trace thickness including a 1 micron Au layer in the bond pad region for improved wire bonding. Figure 68 shows a close-up of the bond region of a thermally imaged cable from first test runs. The accuracy of the line patterning is remarkable and Dyconex is confident they will achieve the challenging goals.

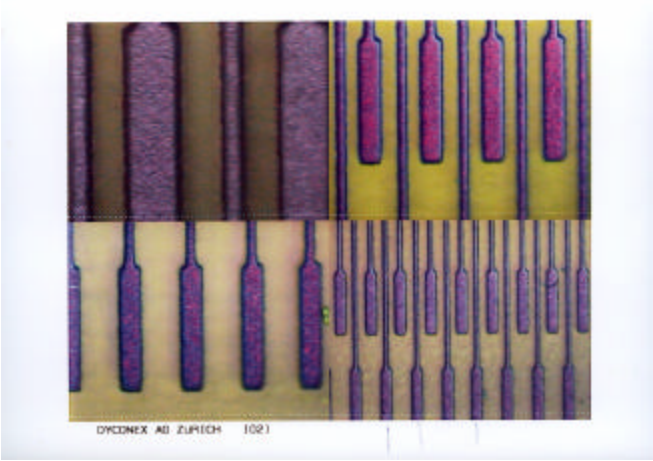


Figure 68 - Closeup of the bond pad regions of first test analog cable. The photograh (courtesy of Dyconex AG) shows four different magnifications of a 50 micron pitch prototype.

First samples of two functional prototype cables have been manufactured recently (end of September). They will be optically inspected and electrically tested. The final ordered engineering sample of 5 - 10 flex circuits with the final gold plated bonding pads and the protection coat are due to arrive at Fermilab for evaluation late 2001.

As a fallback solution, Dyconex proposed a cable fabricated by using two single-laminated Kapton foils, each with 100 um pitch. They will then be adhered together with an offset of 50um so that an effective bonding pitch of 50 um is created. We will also leave open a possibility to use analog cable from KEYCOM, a vendor targeted by CDF.

6.4 Hybrids

This section describes the hybrid design and related electrical issues for the stave design. The proposed beryllia hybrids minimize the amount of material in the detector and are a well established technique used previously in a number of experiments.

Commonly, the circuits connecting the SVX chips to the low mass jumper cable are called "hybrids." The hybrids will be based on the fine pitch thick film etched technology successfully used by CDF in the innermost Layer 00 for alumina substrates and by the CLEO microvertex detector [1] for beryllia substrates. In our case, the 380 micron beryllia substrate will be used to reduce the amount of material in Layers 1 through 5 where the hybrids will be mounted directly in the sensitive volume. For Layer 0 which has off-board hybrids at higher Z, the material issue is of less importance. However, beryllia ceramic is preferred here because of its significantly better thermal conductivity with respect to alumina. Thick film deposition and etching is a mature technology allowing for a minimal feature size of 50 micron. Multi-layer designs are routinely achievable. We have identified CPT Inc. of San Diego as our potential vendor. Despite the fact that they are the only vendor we presently know that will work with such beryllia hybrids, they have successfully produced similar hybrids for CDF and CLEO and we feel confident using them.

There are four types of hybrids in the proposed design. Two of them are 10-chip double-ended versions for Layers 2 through 5: one for axial sensors and one for stereo sensors. Others are a 6-chip double-ended version for Layer 1 and a 2-chip version for Layer 0.

Figure 69 shows possible layouts for the axial 10-chip hybrid and the 6-chip hybrid.

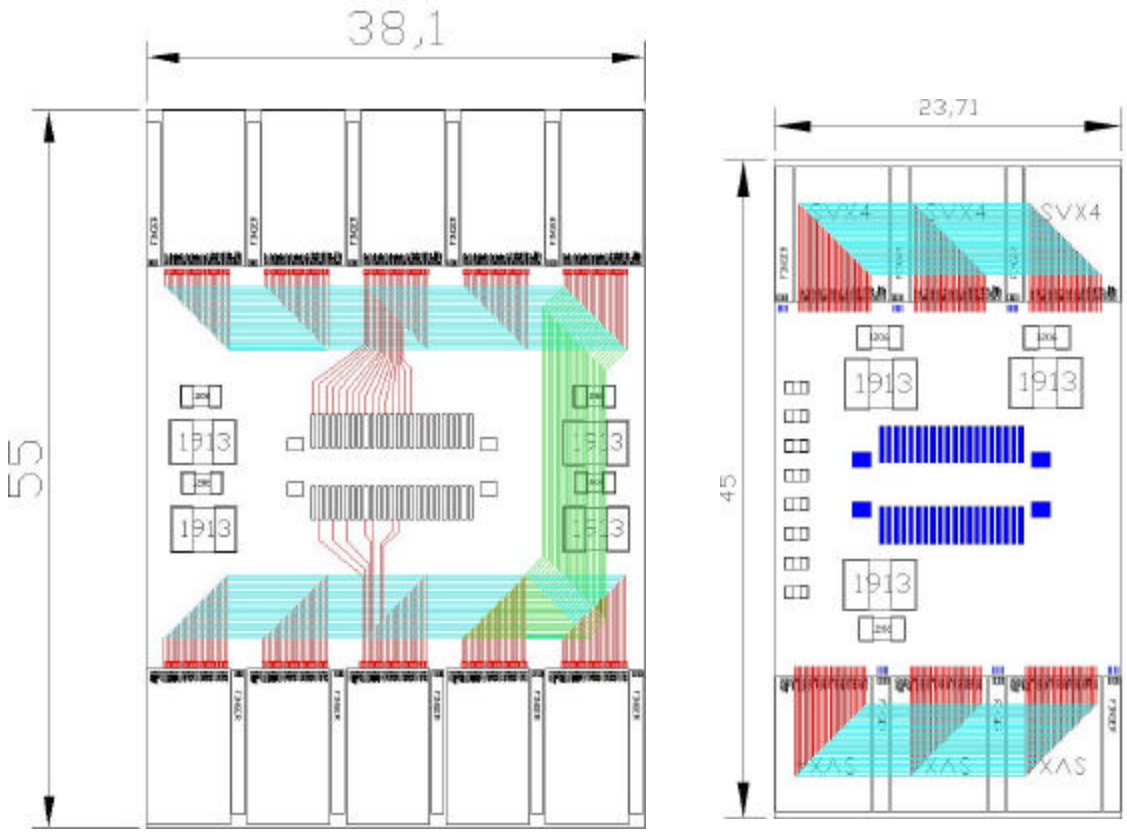


Figure 69 - Double-ended hybrid design with two sensors sharing a common readout cable. The axial 10-chip hybrid (left picture) and the 6-chip hybrid(right picture) are shown.

In addition to providing a secure mount for the SVX chips and cable connector, the hybrids also have capacitors for bypassing the analog and digital voltages and the detector bias. The low mass flat cable connects to the hybrid using an AVX type 5087 connector plug and receptacle. These are 0.5mm pitch low profile connectors with a maximum height of 2.7 mm above the surface of the hybrid. A 50-pin connector will be used for the 10-chip hybrid and a 40-pin connector for the 6-chip hybrid. The CDF SVX detector uses similar connectors with a very low failure rate. Placement of the connector on the hybrid allows for easy testing of hybrids with and without attached silicon sensors during all phases of the hybrid and stave production. This is essential for the modularity of the design and quality checking during stave production. The extra material introduced by the connector is relatively small and is crossed by particles only after two precise measurements in Layers 0 and 1. The 2-chip hybrid for Layer 0 does not have room in the radial dimension for a connector. In this case, the digital jumper cable is soldered directly to the hybrid.

The SVX control signals and readout bus lines are routed from the connector to the SVX4 chips via 100 micron wide traces. The traces stop near the back edge of each chip where they transition into gold-plated bond pads. Aluminum wire bonds connect these pads to the bond pads on the chips. The power traces will be routed from the connector on a power plane, and there will be a dedicated ground plane in the hybrid. The total number of layers is 6. We are also investigating a possibility to route the digital bus under the SVX4 chips as shown for the 6-

chip hybrid in Figure 69. Traditionally, the bus is routed near the chips, as for the 10-chip hybrid layout in the same figure. This new approach allows the reduction of the total hybrid length from 55 to 45 mm.

Since the SVX4 chips have their power bond pads on the side of the chip a small copper on alumina circuit board called a "finger" is placed next to each chip, which routes the power and ground to the region adjacent to the back edge of the chip. This finger facilitates easy wire bonding since its height is nearly the same as the SVX4 height. A second wire bond connects each finger power trace to the hybrid proper. This finger also provides high frequency close-up bypassing capacitance for the chip voltages.

6.5 Cables, Adapter Card and Interface Board Overview

A primary goal of the Run 2B readout chain design is to preserve as much of the Run 2A electronics and cable plant as possible. In particular, we want to keep: 1) the Interface Boards (IBs), located at the base of the central calorimeter, that relay digital signals between the sequencers and the SVX4 chip, supply both low-voltage power and high-voltage bias, and monitor current and temperature; 2) the high-mass cables, consisting of 3M 80 conductor cables and parallel coaxial clock cables that run from the IBs to Adapter Cards on the calorimeter face. Because of the complexity of these IBs, any required changes beyond the scope of component replacements or hand-wired jumpers will likely mandate complete replacement. Also, the space for connectors on the IB face is saturated. A required line count into the IB exceeding that available on the 80-conductor cables could not be accommodated.

As described below, the present design aims to preserve the IBs by replacing the Run 2A passive Adapter Cards on the calorimeter face with active ones that translate between single-ended (IB) and differential (SVX4) signals, and that also regulate supply voltages. The long (up to 2.7 m) Run 2A low-mass cables, which do not have differential-signal capability, will be replaced with new cables comprised of Twisted Pairs connected by small Junction Cards to new, relatively short low-mass Digital Jumper Cables. Feasibility studies showed that DØ could not use the Honeywell transceiver chip that CDF uses in its design [2].

Remaining unresolved issues mostly involve power, bias voltage, and monitoring:

1. The SVX4 chip demands variable supply currents averaging twice those of the SVX2, but this chip can be damaged by over-voltages in excess of 0.25 V. Although the varying voltage drop along the high-mass cables will be handled by the regulators on the Adaptor Cards, there is an additional variable drop along the inner part of the cable path. Whether this will be addressed by brute force (lots of copper), voltage-sensing lines, or a combination, is under study.

2. Layers 0 and 1 require up to 1000 volts of sensor bias. Neither the high mass cables nor thin flex Jumper Cables can reliably stand off 1000 V, so a separate HV wiring path, probably without connectors, will be required for these layers.

3. A better temperature-monitoring scheme, requiring 4 rather than 2 lines per hybrid, is desired.

6.6 Digital Jumper Cables

888 Digital Jumper Cables will carry digital signals and power between the hybrids and the Junction Cards, where they connect to the Twisted-Pair Cables. Jumper Cables will be flex-circuit striplines similar to the low-mass cables used in Run 2A, which minimize the amount of material in the sensitive volume. Signal traces ~0.15 mm wide will be located on one side of a Kapton dielectric, and broad voltage supply and ground traces on the other side.

The maximum required length of the Jumper Cables depends on the location of the Junction Cards; if these are placed at the ends of the support barrels, it is approximately 57 cm. However, access to the Junction Cards may mandate their placement at larger |z|, requiring Jumper Cables up to ~100 cm long. At least two vendors (Honeywell and Basic Electronics Inc.) are known to have capability for flex of this length. Flex width and thickness will be approximately 16 mm and 0.25 mm, respectively. Subminiature connectors, AVX series 5087 (0.5 mm pitch), will be soldered to pads at both ends for silicon Layers 1-5; for Layer 0 the jumper cable will be soldered directly to the hybrid.

Jumper cables will carry, at minimum, 11 differential signal pairs (22 lines), 5 single-ended signals, and two supply voltages and their ground returns. For Layers 2-5 they will also carry lines for sensor high voltage bias and ground and probably lines for voltage sensing. The differential signal lines will be configured as pairs of stripline traces over a ground plane, and can easily be matched in impedance to the 100-ohm twisted pairs. Although it will be difficult to achieve impedance as high as 100 Ohms in the 5 single-ended lines, these signals are slow. Reflections in these lines will probably be tolerable, but will be measured extensively in prototype setups.

Jumper cables for Layers 2-5 will have miniature 50-pin AVX connectors on both ends. This connector will accommodate the 22+5 signal lines and 12 power connections (3 contacts each for 2 voltages and their 2 grounds), the 300 V bias line and its ground return (with 3 empty positions between), and up to 6 monitoring lines. For the Layer 1, there will be room for only a 40-pin AVX connector. Detector bias voltage and its return, and also any required monitoring lines, will have to be connected by soldered jumper wires from pads on the flex to the hybrid or brought on separate wires.

6.7 Junction Cards

Junction Cards have the primary function of connecting jumper cables with Twisted-Pair Cables that lead to the Adaptor Cards. The allowed size of these cards is approximately 25x50 mm. Junction Cards must be mechanically robust and mounted securely, with all attached cabling stress-relieved whenever possible.

The Twisted-Pair Cables can be soldered to the Junction Cards to increase mechanical strength and eliminate an expensive connector; Junction Cards will thus effectively be extensions of the Twisted-Pair Cables.

Connections to the Digital Jumper Cables will be primarily through AVX 0.5 mm pitch connectors. The Junction Card for Layers 2-5 has two 50-pin AVX connectors on one side and two of the same connectors on the reverse side. The junction card for Layer 1 has three 40-pin AVX connectors on one side, and the junction card for Layer 0 has six 40-pin AVX connectors on one side. In addition to lines on the Jumper Cable from the hybrid, there will also be four separate input lines for "bridge" temperature sensing from each hybrid. In the case of 40-pin inputs, separate provision will also be required for sensor bias and its ground return, and likely also for voltage monitoring (see Jumper Cable section).

Unresolved issues for the Junction Cards include:

1. Placement - Although it is desirable to mount them on the ends of the support barrels, hand access (e.g. for plugging in connectors and/or for making soldered connections on the SVX side) may require a location at higher |z|, such as the near the present Run 2A H-disks.

2. Handling of temperature-sensing (RTD) lines - Present plans call for these lines to be separate from the digital Jumper Cables, but to arrive at the Junction Cards. How they will connect, and whether these signals can be accommodated farther upstream in the high-mass cables and in the Interface Boards, has not been resolved.

3. Additional bypassing capacitors - It is desirable for the Junction Card to include additional bypass capacitors for smoothing out AVDD and DVDD voltages, since there is limited space for large capacitors on the hybrids.

6.8 Twisted Pair Cable

The Twisted Pair Cable, approximately 2.4 meters long, connects the Junction Cards and Adapter Cards. The cable is soldered to the Junction Card on one side and is terminated by a connector on the Adapter Card side. Mass is not a major physics issue because the cable is outside of the tracking volume. The total outer diameter of a Twisted Pair bundle can be as small as 5-6 mm.

The twisted pairs were chosen because 11 of the signals used by the SVX4 chip are differential. The 5 slower single ended lines will also use twisted pairs. The cable assembly has 2 power lines and their returns, 1 HV line and its return, 15 signal twisted pairs, 4 or more temperature sensor twisted pairs, and probably 2 voltage sensor pairs. The clock signals can be transmitted either via a shielded twisted pair or via two coaxial cables in the same assembly. Three versions of the Twisted Pair Cable are envisioned (Layer 0, Layer 1, Layers 2-5) depending on the HV and power requirements. The thickness of the power lines depends on whether the "brute force" or "regulator" solution is chosen for the problem of voltage drops. If the former is chosen, the cables get quite heavy, in total about 27 kilograms of copper for each detector half, posing mechanical problems.

A similar dense twisted-pair cable bundle is under development by AXON Cable for the ATLAS experiment at CERN. We have discussed with AXON Cable the possibility of producing cables for DØ; our specifications can be met within reasonable cost. Other vendors will be contacted.

6.9 Adapter Card

The existing passive adapter cards are mounted on the north and south faces of the calorimeter. To fit in the available space, their maximum dimensions are 58x83 mm. For Run 2B, these cards will be replaced by active Adapter Cards to: 1) translate single-ended TTL logic from the Interface Cards to differential signals to and from the SVX4; 2) regulate the voltage of the two SVX4 power lines.

A preliminary schematic for the Adapter Card is shown in Appendix 6.C. A suitable candidate for converting between single-ended and differential signals is the SN65LVDM1677 from Texas Instruments, a 16-channel, low-voltage differential transmitter/receiver with internal 100 Ohm termination. Initially we also considered an option with a Honeywell transceiver chip on the hybrid [2] but in the end preferred a simpler solution with commercial components described above.

Each Adapter Card services two channels. Each channel requires an 80-pin mini D connector and two miniature coax connectors to interface with the 80-conductor high mass cable and clock coaxial cables, and two output connectors, yet undefined, with at least 40 pins, on the Twisted Pair side. Because of space limitations, a daughter card is required for the clock connectors.

Two supply voltages (AVDD for analog, DVDD for digital functions, each 2.5 volts regulated) will be provided to the SVX4, and an additional 3.3 volt supply is required for the active components on the Adapter Card itself. All supply voltages will be enabled by circuitry on the Interface Board. Both AVDD and DVDD voltages must be regulated to within 250 mV at the adapter card. An understanding of the current swings in the SVX4 is required for final choice of a voltage regulator; the preliminary schematic shows a LT1087 for this part. Use of sense lines may be required if current consumption between modes changes quickly and significantly.

Decoupling and filter networks will be required on the 300 V sensor bias lines for Layers 2-5. The 1000 V bias for Layers 0 and 1 will not be transmitted through the Interface Board.

Adapter Card testing will best be done with the first SVX4 chips. A full test stand with the entire upgraded data path should be implemented immediately upon availability of useful chips. Mock-ups of signal conditions for parts of the SVX4 may be useful in exploring signal levels, supply conditioning, and cross-talk levels.

6.10 Interface Board

In order to avoid the considerable expense of designing and building new Interface Boards, the existing IBs must be recycled and all new features for Run 2B must be incorporated into the active Adapter Card (AC). As stated in the Overview section above, any required changes beyond the scope of component replacements or hand-wired jumpers will likely mandate complete replacement.

The IB detector bias distribution was tested to + 200 V, -100 V (including the switching relay) and should be safe for 300 V for silicon Layers 2-5. Bias cables for Layers 0-1 (up to 1000 V)

cannot go through either the IB's or the existing high-mass cables. Suitable routing is under study.

Required changes on the IB which have been identified to date include:

1. Replacing data line terminations (24 resistor changes per channel)
2. Probable changes in control line termination, and in the clock equalizer circuit
3. New set points for current and temperature trips
4. Reprogramming of 5 PLDs
5. Changes to priority-out signal threshold and hysteresis (this line was underdriven by the SVX2 chip)

The total number of changes is about 200 per interface board.

6.11 Sequencer

The firmware in the sequencer needs to be adjusted for the difference between the SVX4 chip operating in the SVX2 mode and real SVX2 chip. The changes are rather straightforward and imply remapping of the SVX2 lines to SVX4 lines. The required remapping was shown in the section describing the SVX4 chip.

6.12 Low Voltage Distribution

Currently VICOR switching power supplies [3] are used to provide power for the SVX2 chips and Interface Boards. For Run 2B we intend to preserve those supplies and the distribution scheme through the Interface Boards.

The massive power lines from the VICOR supplies are split between different channels in the fuse panel. After the individual protection fuses, the power is distributed to the custom J1 backplane of 9U x 280 mm custom crates. The J2 and J3 backplanes of the crates provide connectors for the cable runs to the sequencers, while J1 contains connectors for low-voltage power for each Interface Board and up to eight dependent silicon hybrids, the 1553 connector and bus (used to monitor the SVX4 power and current, and hybrid temperature), and a connector to bring in 16 bias voltages and returns for eight hybrids.

We are investigating the feasibility of replacing the J1 backplane. This would have the benefit of eliminating the existing fuse panels; these panels are time-consuming to wire, and contain ~150 fuses which experience has shown to be somewhat unreliable due to oxidation of contacts. A small number of fuses would still need to be placed for safety reasons on J1 and perhaps on the IB (replacing existing ferrite beads there). Another advantage of J1 replacement is that remote sense from the external power supplies would go to the J1 bus instead of stopping at the fuse panel. We will have more space at the backplane because a 34-pin bias connector can be replaced with a smaller one, since the new single sided detectors only need one bias voltage.

The feasibility of this scheme must be established, and mechanical and electrical layouts need to be done. The Interface Board side of the backplane would be unchanged.

6.13 High Voltage Distribution

Reliable high voltage operation is crucial to ensure the increased radiation tolerance of the new Silicon Tracker. Operation at voltages up to +1000 V is necessary for the Layers 0 and 1 and up to +300 V for the Layers 2 through 5. Despite the fact that Run 2A silicon detectors require operating bias voltages only within ±100 V, the specifications of the existing Run 2A HV power supplies are adequate for Run 2B detectors. More HV channels are needed to bias larger number of sensors. The most straightforward upgrade path for the HV system is increasing of the number of the existing channels.

The high voltage bias will be applied to the backplane of the single-sided silicon sensors. For 10-chip hybrids the high voltage will arrive at the hybrid on the Jumper Cable and will be routed to a side pin of the AVX connector. Two neighboring pins will be removed to ensure a safe distance to the nearest ground. The bias voltage will be brought to the sensor backplane with a foil wrapped around the sensor edge and glued to the backplane with a conductive silver epoxy. The foil will be insulated from the sensor edge and from the outside with a 50 micron kapton tape. For the Layers 0 and 1 a separate wire will be used to bring the bias voltage to the hybrid. For Layer 1 the backplane connection will be provided similarly to the 10-chip hybrids while for Layer 0 the bias voltage will be fed to a line on the analog cable and then will be connected to the backplane of the sensor near the end of the cable.

For all layers one HV channel is used per hybrid. Therefore, each sensor in Layer 0, two sensors in Layer 1 and two, three or four sensors in Layers 2-5 will share the same HV channel. Conducting pieces bridging together two backplanes will provide the connection between the sensors when required. The total number of HV channels needed is 888. A possibility of bias splitting between two or more hybrids in the outer layers can be considered to reduce the number of HV channels.

In the Run 2A system, bias voltages are supplied from a BiRa VME 4877PS High Voltage Power Supply System [4]. The system utilizes the three HVS power supply types shown in Table 9. Overvoltage protection is provided through trim potentiometers located on the front panel of the modules.

Table 9 - HVS power supply types used in the DØ Run 2A silicon bias voltage system.

HVS type	max output voltage, kV	max output current, mA	number of channels
HVS5.5P-1	+5.5	2.3	116
HVS5.5N-1	-5.5	2.3	152
HVS2P	+2.0	3.2	116

Each of the eight VME crates in the Run 2A HV system holds a Power PC controller and six motherboards containing eight Bi Ra power supplies each. Power to the VME crates is delivered from Lambda power supplies. A Run 2B system with 888 HV channels will require 111 motherboards, as well as 19 VME crates with controllers and power supplies.

The Run 2A fanout and breakout boxes will need to be replaced. The fanout boxes are used to split HV channels between different HDIs and to provide hardware protection against accidental application of HV higher than 150 V. The breakout boxes are used to distribute HV to the Interface Boards and to transfer temperature signals from the Interface Boards to interlock control systems.

It was checked that the HV path through the Interface Board and 80-conductor cables can sustain up to 300 V and, therefore, can be preserved in Run 2B for Layer 2-5 bias distribution. The design goal for HV distribution for the inner two Layers is operation at 1000 V. In this case, the HV cabling needs to bypass the Interface Board and go directly to the Adapter Card via a separate cable.

6.14 Performance

Increased luminosity in Run 2B will result in high occupancy in the detector especially for the inner layers. This has several implications for the readout performance. Two areas of concern, the SVX4 dynamic range and the detector readout time, were addressed in our simulations with results presented in this Section.

The charge-sensitive preamplifier of the SVX4 chip integrates incoming signals and, therefore, needs to be reset regularly to prevent saturation. The saturated preamplifier will result in inefficiency of the detector. The reset time in SVX4 is equal to several hundred nano-seconds. Usually the resets are performed during the Tevatron abort gaps, which are periods of time within one revolution without collisions. Along with other modifications the high luminosity regime of the Tevatron operation in Run 2B will include reduction of the available abort gaps to possibly one per revolution. The current 36 bunches x 36 bunches operation allows for 3 abort gaps per revolution.

The full GEANT simulation with the Run 2B geometry discussed in CHAPTER 9 - and realistic clustering in the silicon has been used to estimate charge accumulated per strip after 450 minimum bias events. A scenario of 150 beam crossings before a reset with 3 minimum bias interactions per beam crossing was assumed. Figure 70 shows the charge per strip in the innermost layer after 450 minimum bias events. The left plot corresponds to the sensors in the central (closest to z=0) barrels. The right plot corresponds to the sensors in the end barrels. The central sensors are crossed by a larger number of particles while the incidence angles are shallower for the end sensors allowing for a larger deposited charge. As shown by arrows in both cases about 1% of strips will receive charge in excess of approximately 100 fC, which corresponds to 25 minimum ionizing particles. The dynamic range of the SVX4 chip was chosen to be 200 fC, leaving some margin for high luminosity operation. The expected inefficiency caused by the preamplifier saturation is expected to be less than 0.1%.

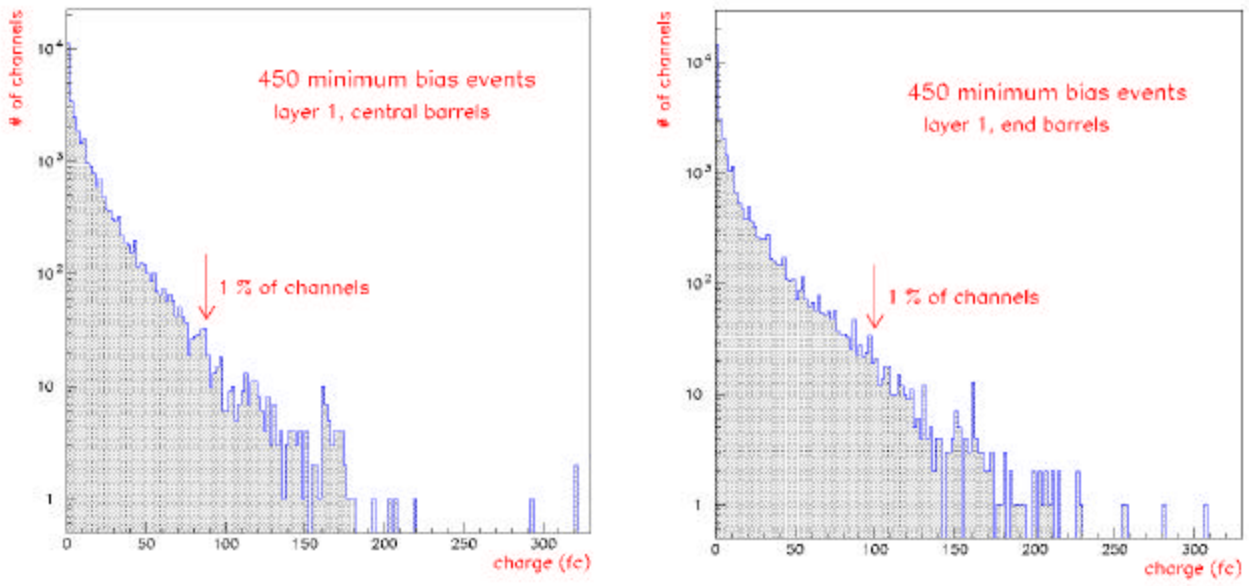


Figure 70 - Charge per strip in the innermost layer (labeled layer 1 in the figure) after 450 minimum bias events. The left plot corresponds to the sensors in the central, closest to z=0, barrels. The right plot corresponds to the sensors in the end barrels.

Another important performance issue for data acquisition is the readout time. A p-pbar interaction triggered for readout will be accompanied by several minimum bias interactions. To investigate a wider range of Level 1 triggers, several simulated samples were used: minimum bias, two jet and WH events. The maximum number of strips per readout cable in a layer was determined for each event. This number corresponds to the slowest chain of readout in this layer and is relevant to estimate the readout time for the detector and the associated dead time. The number of hit strips has been scaled by appropriate factors to account for the closest neighbors that normally are also included in the sparse mode readout. The factors were determined from the cluster size distributions and were typically around 1.7 for the cases without noise and 2.8 for the cases with noise. Figure 71 shows the maximum number of strips per readout cable as a function of radius for minimum bias events (left plot) and QCD two jet events (right plot). Each layer corresponds to two points in those plots from different sublayers. Four different cases were considered: without noise for the two thresholds of 4 and 5 ADC counts, and with noise (rms 2.1 ADC counts) for the same thresholds. The average simulated signal was equal to 20 ADC counts corresponding to a S/N ratio of 9.5. Figure 72 shows the maximum number of strips per readout cable as a function of radius for WH + 0 minimum bias events (left plot) and WH + six minimum bias events (right plot).

Comparison of the inner three layers with the highest rates suggests that Layer 1 with 6 chips in the readout chain and Layer 2 with 10 chips will operate in similar conditions for all types of events. Layer 0 with 2 chips in the readout chain has rates a factor of 2 lower. However, this layer will experience the worst radiation damage and, as a result, a lower S/N. The effect of the noise on occupancy depends on the threshold. For the threshold over noise ratio equal to 2.4 the deterioration of S/N from 9.5 to 8 increases the maximum number of readout strips by 40% in Layer 0, by 50% in Layer 1 and by 75% in Layer 2, all for two jet events. The largest increase is observed in the 10-chip readout chain of Layer 2 due to the simple fact that the number of noisy

strips is proportional to the number of chips. A lower S/N ratio in the innermost layer 0 can easily increase the number of readout strips by a factor of two and make its rate comparable to the Layers 1 and 2. As a result of these simulations, we feel it is prudent to daisy-chain only two chips in Layer 0 and leave a safety margin to accommodate higher noise occupancy in this layer after irradiation.

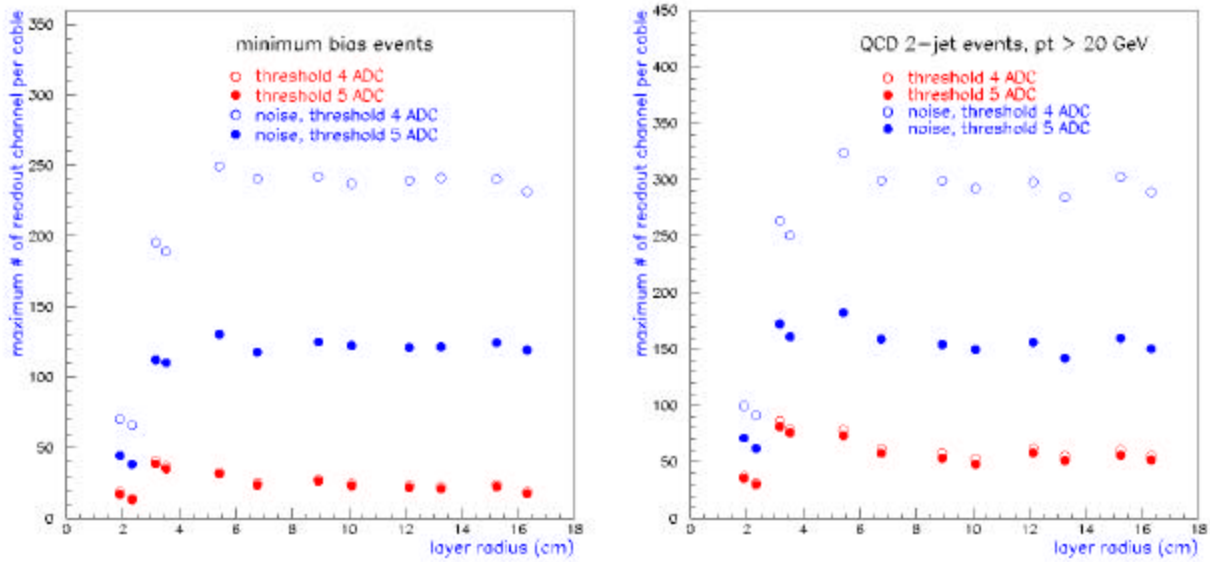


Figure 71 - Maximum number of strips per readout cable as function of radius for minimum bias events and QCD two jet events

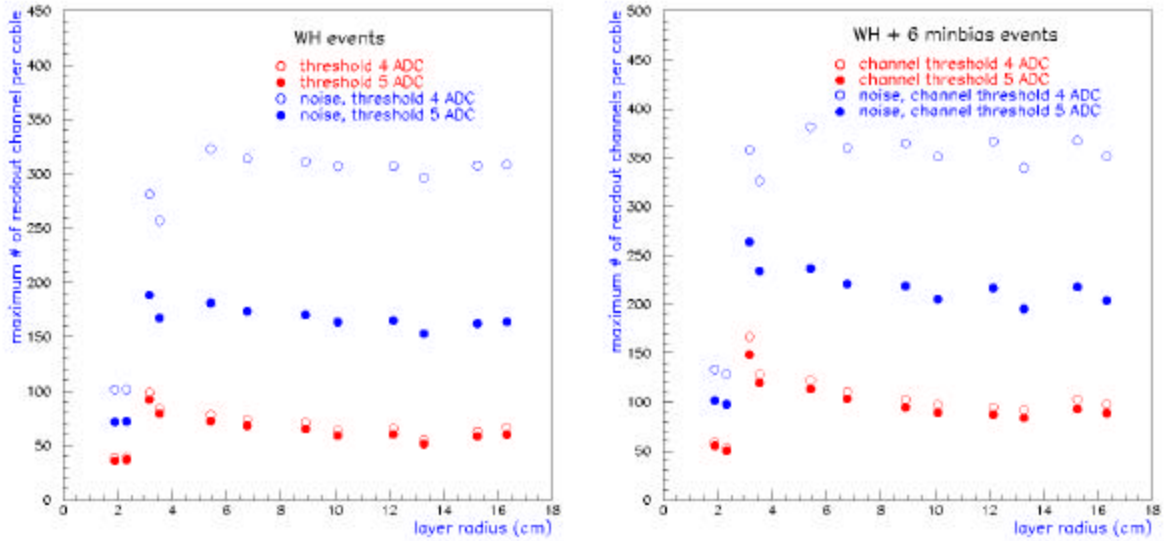


Figure 72 - Maximum number of strips per readout cable as function of radius for WH + 0 minimum bias events and WH + 6 minimum bias events.

The above information is useful for the evaluation of the deadtime. The readout of SVX4 is driven by a 53 MHz clock. Two bytes of data per channel (address and amplitude) require two clock cycles. This gives a total readout time of an SVX4 chip of about 4 microseconds for a

typical occupancy of 100 strips. The deadtime will be determined by the SVX4 digitization time, readout time and the pipeline reset time after the readout. Though the correct calculation should combine information from all silicon layers and all levels of the DØ trigger in a queue analysis, essentially one buffer structure of the DØ data acquisition makes a simple rough estimate possible. The total deadtime can be estimated as

3 (digitization) + 4 (readout) + 4.2 (pipeline reset) = 11.2 microseconds

At 10 kHz Level2 trigger input rate, corresponding to 100 microseconds between Level_1_Accept signals, the deadtime will be equal to approximately 11.2%. The deadtime and the readout time are acceptable for the DØ data acquisition system and in particular for the Silicon Track Trigger at Level 2.

6.15 Appendix 6.A

Preliminary adapter card input connector (80 conductor input cable from the Interface Board).

Pin #	Function	Pin #	Function
1	Secondary Bias A	41	NC
2	GND	42	NC
3	GND	43	Primary Bias A
4	GND	44	3.3 V
5	Temperature A	45	3.3 V
6	VCAL A	46	3.3 V
7	D7 A	47	3.3 V
8	D6 A	48	2.5 V Unreg AVDD A
9	D5 A	49	2.5 V Unregulated AVDD A
10	D4 A	50	2.5 V Unregulated AVDD A
11	D3 A	51	2.5 V Unregulated AVDD A
12	D2 A	52	2.5 V Unregulated AVDD A
13	D1 A	53	2.5 V Unregulated AVDD A
14	D0 A	54	2.5 V Unregulated AVDD A
15	Priority In A	55	2.5 V unreg DVDD A
16	Mode 0 A	56	2.5 V unreg DVDD A
17	Mode 1 A	57	2.5 V unreg DVDD A
18	Change Mode A	58	2.5 V unreg DVDD A
19	DValid A	59	2.5 V unreg DVDD A
20	Priority Out A	60	2.5 V unreg DVDD A
21	GND	61	3.3 V
22	Temperature B	62	3.3 V
23	VCAL B	63	3.3 V
24	D7B	64	3.3 V
25	D6 B	65	2.5 V Unregulated AVDD B
26	D5 B	66	2.5 V Unregulated AVDD B
27	D4 B	67	2.5 V Unregulated AVDD B
28	D3 B	68	2.5 V Unregulated AVDD B
29	D2 B	69	2.5 V UnregulatedAVDD B
30	D1 B	70	2.5 V Unregulated AVDD B
31	D0 B	71	2.5 V Unregulated AVDD B
32	Priority In B	72	2.5 V unreg DVDD B
33	Mode 0 B	73	2.5 V unreg DVDD B
34	Mode 1 B	74	2.5 V unreg DVDD B
35	Change Mode B	75	2.5 V unreg DVDD B
36	DValid B	76	2.5 V unreg DVDD B
37	Priority Out B	77	2.5 V unreg DVDD B
38	Primary Bias B	78	GND
39	NC	79	GND
40	NC	80	Secondary Bias B

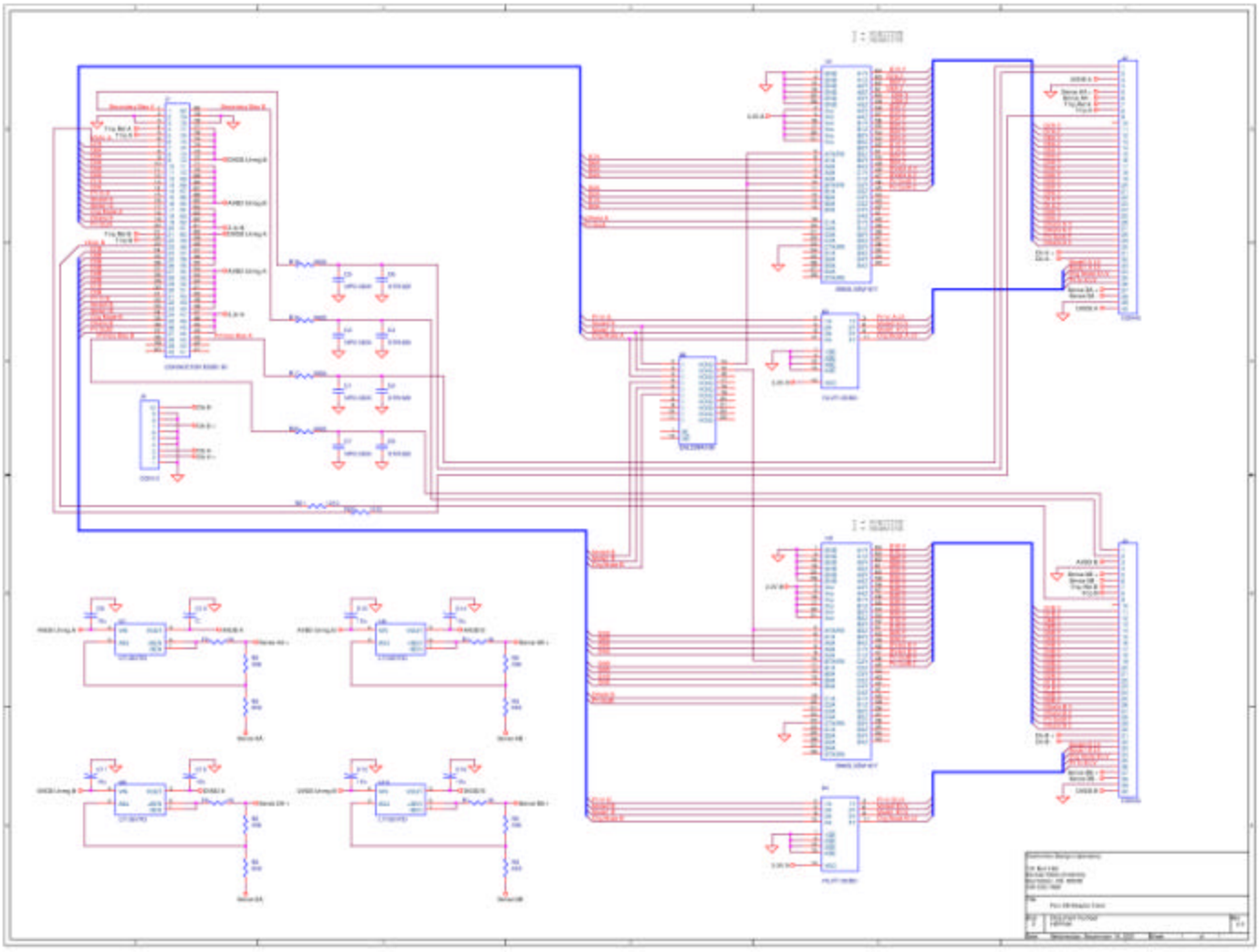
6.16 Appendix 6.B

Preliminary adapter card output connector pinout

Pin #	Function	Pin #	Function
1	Primary Bias	21	D2+
2	Secondary Bias	22	D2-
3	AVDD	23	D1+
4	GND	24	D1-
5	Sense A +	25	D0+
6	Sense A -	26	D0-
7	Temperature	27	DV+
8	Temperature Return	28	DV-
9	VCAL	29	Priority Out +
10	NC	30	Priority Out -
11	D7+	31	Clock +
12	D7-	32	Clock -
13	D6+	33	Mode 0
14	D6-	34	Mode 1
15	D5+	35	Change Mode
16	D5-	36	Priority In
17	D4+	37	Sense D +
18	D4-	38	Sense D -
19	D3+	39	GND
20	D3-	40	DVDD

6.17 Appendix 6.C

Preliminary schematic for the adapter card



[1] Nucl.Inst.Meth. **A435**, 9-15, 1999

[2] DØ Note 3905, "Feasibility Testing of the Radiation Hardened Transceiver Chip for use in the DØ Run 2B Upgrade Project at Fermilab", John Ledford et al.

[3] 4 kw MegaPAC AC-DC Switcher, Vicor Corporation, Andover, MA.

[4] Model VME 4877PS High Voltage Power Supply System Manual, March 1988, Bi Ra Systems, Albuquerque, NM.

CHAPTER 7 - PRODUCTION AND TESTING

In this section we describe how we plan to build and test detector modules starting from individual components and resulting in working detectors on staves. We will try to adapt steps used in the very successful production and testing effort DØ organized during the construction of the Run2A Silicon Microstrip Tracker. The essential building blocks of a detector module are the silicon sensors and the readout hybrids. Each component is tested as described below before it is assembled into a module. After the assembly the modules are tested again before they are mounted on staves. A detailed description of the stave assembly and installation is included in the Section CHAPTER 5 - . Testing of staves and of the full readout system are also included below.

7.1 Silicon Sensor Testing

To ensure high quality of the silicon sensors DØ plans a series of quality assurance tests to be performed by the supplier and by DØ. The manufacturer will perform the following tests:

7.1.1 On each sensor

- Measure leakage current as a function of reverse bias up to 800 V at room temperature ($T = 21 \pm 1°C$) and RH < 50%.
- Visual inspection at a specified magnification for defects, opens, shorts , and mask alignment (better than 2.5 μm)
- Depletion voltage measurement either by the measurement of the capacitance between back-plane and the bias ring at 1 kHz frequency as a function of reverse bias, or by similar measurement performed on a test diode produced on the corresponding wafer.

7.1.2 On each strip

- Capacitance value measurement and pinhole determination
- Leakage current at Full Depletion Voltage (FDV) and Room Temperature (RT)

Based on these tests, we define a “bad channel” as follows:

- Pinholes – current through capacitor >10 nA at 80 V and RT
- Short – coupling capacitor >1.2 times the typical value
- Open – coupling capacitor <0.8 times the typical value
- Leakage current above 10 nA/strip at FDV and RT

Strips with bias and interstrip resistance values outside the limits specified above shall be counted towards the bad channel list. The total number of bad channels must not exceed 1%. In addition, we plan to perform the following measurements on the test structure: Poly resistor value, sheet and implant R, and coupling capacitor breakdown voltage.

The corresponding quality control data of the applied tests from the supplier shall be provided together with each sensor. Our goal is to keep all the information in a centralized production database, as explained in the next chapter. DØ plans to verify the provided data on every pre-production sensor (total of 200 sensors) and on 5-10% of the production sensors, which corresponds to ~220 sensors. Fermilab and three additional off-site sensor-probing sites are being set up for this purpose. Each setup consists of a fully automated probe station mounted on a vibration free table and enclosed in a dark box. Each setup is housed in a clean room environment and the probe station is operated using Labview software. The estimated average throughput of each facility is four silicon sensors per day.

7.2 Hybrid Production And Testing

The hybrids are beryllia substrates with SVX4 chips, fingers, and passive components mounted on them. The SVX4 chips will be tested as described in Section xx before they are released for use in the hybrid production line. The fingers, which are mounted between the chips on the hybrid, will also be measured to assure they have the correct dimensions and capacitance values. We will investigate the necessity for testing every bare hybrid substrate during production, but believe that probe stand setups will be needed at least in the prototyping stages. Once all of the components have been released for production, they are sent to a vendor for stuffing, mounting, and wirebonding onto the hybrid.

The hybrid is now ready to undergo an initial functionality test that includes both electrical and mechanical qualification. A thorough visual inspection of the stuffed hybrid will certify that the components were mounted correctly and that the wire bonds were not damaged during shipping. Pull tests of wire bonds will be done initially on each hybrid. If no problems are encountered, the number of pull tests done may be relaxed to a small fraction of hybrids. In addition, procedures will be developed to ensure that the hybrids have the required flatness, required for mechanical considerations. We may need to glue a backing to the hybrid at this time.

A testing cable will be connected to each hybrid to facilitate electrical testing. A short electrical functionality test will be done in which the hybrid is connected to a stand alone-based test stand that will be used to download to the SVX4 chips and read out the hybrid. Hybrids that fail any step of the functionality test will be sent to the repair team, for diagnosis and repair. Hybrid testing and repair is expected to proceed off-site during production to alleviate the load on the Fermilab production line. Hybrids that pass the functionality test will be shipped to Fermilab for the "burn-in" phase.

Extensive electrical tests (burn-in) will be carried out on the hybrids over a period of 72 hours during which they will be kept powered at room temperature. Pedestal and noise will be measured in data and cal-inject mode for each channel. Sparse readout will also be tested. Acceptable levels of noisy and dead channels and gain will be defined and each of the hybrids

graded for further assembly. The burn-in time will be evaluated as production progresses to determine whether it can be shortened.

7.3 Module Assembly And Testing

Information about the depletion voltage and the number of bad strips will be provided as input to the testing and assembly group and taken into account when choosing sensors for a particular detector module. Only those hybrids meeting the desired criteria will be matched to silicon sensors and assembled into detector modules. The techniques for assembly of detector modules will be similar to those used in the past by many groups, including DØ. Sensors will be manually aligned with optical feedback from a camera mounted on a coordinate measurement machine (CMM). Once aligned, the sensors will be glued to one another, directly or via a connecting substrate. Reasonable expectations for this alignment are accuracy to a few microns. The hybrid will be glued directly to the silicon sensors in such a manner that the guard rings are not bridged by adhesive, to avoid any performance problems. Methods for this procedure will be prototyped soon.

Wire bonding will then be done between the hybrid and the sensors, and from sensor to sensor for the modules with 20 cm readout segments. The sensor pitch is such that the hybrid to sensor bonding can be done directly from the SVX chips to the silicon sensors without a pitch adapter. The total numbers of wire bonds required for layers 2-5 are 353K sensor-to-sensor plus 860K hybrid-to-sensor, for a total of 1213K bonds. For the longer modules, the sensor-to-sensor wire bonding will be done either before or after the hybrid is mounted. Sensor alignment and sensor-to-sensor wire bonding could therefore proceed prior to hybrid delivery, should that become a production constraint. At several steps of the assembly sequence, the module will be electrically tested, repeating the short functionality test. Malfunctioning modules at any step of the assembly sequence will be sent to the repairs team for diagnosis and repair. We will consider the possibility that the individual modules may require cooling during the diagnostic tests to avoid over heating.

We are investigating the feasibility of using a single fixture for gluing and wire bonding. Adding a cover to the fixture would make it serve, in addition, as the testing and storage box. The advantage of this approach would be to minimize the handling of the detector modules, thus avoiding possible damage.

Completed detector modules will be sent to the debugging team to investigate their performance under HV bias. Pinholes could develop during wire bonding and can be removed by pulling the wire bond between the AC sensor pad and the SVX4 chip preamplifier. Because all our silicon modules use single-sided silicon sensors, we expect the debugging of detector modules to be much less demanding than the one required by double-sided sensors. Once the detector module is operational under high voltage, it will be sent for module burn-in.

The module burn-in test will use a replica of the setup and software utilized during the hybrid burn-in test, with a few additions: first, the modules will be cooled so that they effectively run at a temperature of about 5 to 15 degrees Celsius, depending on detector type. Second, the sensors will be biased at 5V above their depletion voltage as determined from sensor testing. The

information obtained from the module burn-in test on the number of dead and noisy channels, and leakage current at depletion voltage, will be used to assign an electrical grade to detector modules before they are assembled into staves.

A small fraction of detector modules that pass the burn-in test will be sent to the laser test, where they will be placed on an x-y movable table, biased and illuminated with a highly-collimated pulsed IR laser, providing a detailed test of each strip of the detector module in a functional setting.

Our goal is a production rate of 10 detector modules per day. We need a total of 144 L0, 71 L1, 336 10/10, 120 10/20, and 216 20/20 detector modules, and assume 10% additional modules of each type will be needed to complete the tracker. We expect the bottleneck for the production to be the wire bonding, although availability of appropriate size CMM machines and glue setting times are also potential problems. Based on our Run2A experience, we estimate that we will need a maximum of half an hour per detector module to make the silicon-to-silicon and silicon-to-hybrid bonds using the fast 8090 bonders. We assume that one 8090 bonder will be available to DØ for 14 hours per day, which would allow us to produce 28 modules per day. Assuming a 75% efficiency, we arrive to our estimate of a maximum production rate of 20 modules per day. We feel comfortable aiming at a steady production rate of half our absolute maximum capacity, i.e. 10 modules per day. This number is consistent with the number of CMMs available and the number of fixtures assumed for each module type, as detailed in the Mechanical section.

7.4 Production Testing Readout Stands

All the tests performed on readout hybrids and detector modules will use essentially the same type of test stand, based on the Stand Alone Sequencer Board (SASeq), developed at Fermilab. The SASeq based test stands were developed during Run 2A independently from the full DØ readout system. These were relatively inexpensive, which allowed us to replicate them in large quantities and distribute them at various locations at Fermilab and at Universities, long before the final version of the full readout system was available. Using an easily reproducible, relatively inexpensive version of the readout system proved crucial to the success of the production and testing effort. Essentially, two types of test stations were built: burn-in stations, that could operate 16 devices (hybrids or detector modules) at once, and one-SASeq test stand that could read out only two devices at once. A detailed description of the systems can be found in DØnote 3841. We plan to refurbish the existing Run 2A testing stations by reprogramming the stand-alone sequencers (SaSeq) and replacing the adapter cards that interface the hybrids either directly to the SaSeqs or through the Interface Board, which must also be replaced or modified. The existing two burn-in stations will be utilized for hybrid burn-in and will provide for a capacity of 32 hybrids simultaneously.

To achieve the peak production rate, we are planning on a detector burn-in capacity of 80 modules per day. A 1-to-4 relation between maximum production rate and detector burn-in capacity existed during Run 2A, and was appropriate. We will therefore build two new module burn-in stations, each with a capacity of 40 modules. Each burn-in station will provide individual cooling and high voltage to each detector module. An interlock system is needed to shut down power in case of high humidity or high temperature, in order to avoid damage to the

large number of detector modules being tested at once. At the early stages of the production, one of the module burn-in stations can be used to burn-in hybrids.

Software for the fast functionality, burn-in and laser test was developed for the production testing effort during Run2A and will be modified to accommodate the new readout hybrids and module geometry. Detailed bookkeeping of the status and location of each detector module during production is crucial to the task. Detailed information about characteristics of sensors and SVX chips is also needed. We plan to set up a production testing database that would be used as the centralized location for storing information linked to the project.

7.5 Module Installation

Fully tested detector modules will be installed in staves, as described previously. The short electrical functionality test will be repeated on biased detector modules after their installation on staves to assure no damage occurred during the handling. We are investigating the need for cooling the detector modules during this operation to avoid overheating.

Completely tested L2 to L5 detector modules will be installed on staves while the detector module production continues. We are therefore planning on a storage capacity of 25% of the total number of detector modules (plus 10% spares) for layers 2 to 5. We expect the L0 and L1 detector module production will be very advanced before the modules are installed on the support structure; thus we are planning on having the ability to store the totality of the detector modules (plus 10% spares) for layers 0 and 1.

A final fast functionality test of biased detector modules will be performed after the final readout cables are connected to the staves.

7.6 Full System Electrical Test

We plan to test the full readout chain with a small number of full staves through all of the components of the final readout chain. The goal of this test is to understand the full readout system and perform modifications well before the system needs to be operated in the collider. The same idea was behind the so-called 10% test during the production of the Run2A detector. At that time, a large number of components that were eventually installed in the detector were used for the test. Because we are reusing a fair amount of components for Run 2B, we cannot plan on a large-scale full system test like the one we had during Run2A. The cost of the equipment is too high. Nevertheless, we believe that a smaller scale full system test is imperative. We therefore plan to test between 2 and 4 staves with the full readout chain. Appropriate cooling will be provided to the staves to test the components for structural as well as electrical integrity when run at the actual operating temperature. This will ensure that the stave performance is as expected at their nominal operating temperature.

CHAPTER 8 - SOFTWARE

This section describes the software needed for commissioning, calibration, monitoring and online readout of the detector. The offline software effort will follow on from the present Run 2A effort and is not described in this document. For this online software effort, we will use the system developed for Run 2A and upgrade it appropriately for Run 2B where needed. Here we describe this system.

The requirements to the software are mainly determined by the hardware that is used. The SVX amplifier chip requires a set of parameters like the amplifier bandwidth, a threshold for zero suppression and various ADC settings. The delay for the readout is set at the Sequencer Controller module. Each module requires an individual set of parameters. These parameters are downloaded after power up. Special data taking modes, e.g. calibration runs, require a different set of parameters. In addition some parameters might change with time. The most important example is the threshold for zero suppression, which changes with fluctuations of pedestal and noise. Constant monitoring ensures that the download parameters are still correct. It is also necessary for ensuring a constant high data quality and the safety of the detector.

The main components of the SMT online software are the ORACLE database, Graphical User Interfaces for control and monitoring, the Secondary Data Acquisition for calibration and monitoring, and Examine programs, which are part of the offline framework but are used in the online context.

The Online Database for SMT consists of three parts, the Hardware Database, the Electronics Database and the Online Calibration Database. The Hardware Database contains the definition of EPICS process variables (see below). These are required for communication with hardware modules. In addition alarm information is stored which is used for monitoring and the Significant Event System (SES). The Electronics Database contains the complete mapping of the hardware. Every type of readout module has its own table. An individual module is represented by a row in this table. A representation of single channels of modules allows the necessary multiple references between readout modules. The database contains the hardware identification for the modules as well as all the parameters necessary to operate the module. A history mechanism allows one to keep track of changes to the downloaded parameters. One then has knowledge of the parameters that have been used at any time during the data taking period. The Online Calibration Database contains the basic calibration data for each readout channel per calibration run as well as summary information per SVX chip per calibration run. In addition a status word is assigned to each of the readout channels. These databases are implemented using ORACLE, which is software maintained by the computing division at Fermilab.

The Graphical User Interfaces (GUIs) include EPICS as well as other control and monitoring interfaces. EPICS (Experimental Physics and Industrial Control System) is used to communicate with the hardware. A VME single board computer (Power PC MV23xx series) maintains a database of symbolic names which are mapped to one or more hardware addresses. A host computer can access these symbolic names via an EPICS client. The EPICS clients and servers then communicate via the Ethernet network. This system allows an easy implementation of a centralized control and monitoring system with distributed hardware.

The MIL1553 standard is used to communicate with non VME modules. A custom built VME module, the 1553 Controller, is used to access the 1553 bus. The 1553 bus is a robust communication link widely used in commercial and military aircraft. EPICS is used to communicate with the 1553 devices.

EPICS allows periodic sampling of the hardware. Threshold values are used to issue warning or error messages to the Significant Event System (SES). This allows a distributed monitoring of variables locally without the need for a central host. In principle it is possible to implement an immediate response to a monitor value that exceeds a set limit directly on the local machine. Messages of the SES are regularly monitored by the shift crew. These messages are archived as well.

The programming language used to interface the database and the hardware is Python. Python has several advantages:

- Python is an Object-Oriented Language. It therefore allows the use of modern programming techniques.
- Python is a script language. It is compiled to a compact, byte-oriented stream for efficient execution. Program development has fast turn around cycles.
- Python has a convenient to use Tcl/Tk library. The programming of GUIs is simple and fast.
- Python also has a freely available interface to ORACLE databases.
- A Python wrapper around the C-interface to EPICS has been developed by DØ.

Because of these advantages Python has been the choice to develop GUIs for interaction with the database and with the hardware. One of the disadvantages is that the execution speed suffers from the fact that Python is a script language.

A GUI has been developed to interface both the ORACLE database and the hardware. The database is used to determine the mapping of the readout electronics. Each module is represented by one GUI entity. Each entity has two functionalities:

- The parameters for a specific module that are stored in the database can be modified.
- The hardware registers of this module can be accessed.

In addition to providing an interface to single readout modules, global functions acting on a complete readout crate are implemented. These include:

- Complete initialization of a readout chain.
- Recording of a pedestal event.
- Recording of a pulser event.

- Event display.
- Reset of the VME readout crate.
- Switching to the readout of a test pattern.
- Status scan of the bias voltage.
- Switching the power of the readout chips off.
- Processing of calibration runs.
- Status display of all modules belonging to one crate.

Single modules and complete segments of the readout crate can be disabled. In this way every readout component can be tested individually during commissioning.

Additional GUIs are also available:

- Monitoring of voltages, currents and temperatures of all the silicon detectors.
- Monitoring and Control of the bias voltage of the silicon. Each silicon detector has one or two bias voltages that have to be set individually. A database with the HV parameters exists.
- Monitoring of temperatures of the Interface Boards.
- Monitoring and Control of the low voltage power supplies.
- Monitoring and Control of the VME single board computers.
- Security monitoring (water leaks, fire, cooling).

Any EPICS variable can be queried with a frequency of up to 10Hz. Those values are stored on disk. Voltages, currents and temperatures for all the silicon detectors are stored that way. In addition, voltages and currents from the power supplies are monitored. A tool to retrieve and to display this information exists.

The calibration of the silicon detectors is done using the Secondary Data Acquisition (SDAQ) system. SDAQ is integrated in the DØ DAQ framework. It uses the DAQ components Coordinator (COOR), Data State Manager (DSM) and Data Merger (DM) but is distinguished from the Primary Data Acquisition by the fact that the Level 3 Trigger is not used. The data collection and data analysis is done locally for every readout crate on the single board computer, the Input/Output Controller (IOC). The summary of the calibration result, i.e. pedestal and gains and the corresponding uncertainties for each SMT channel, is sent at the end of the calibration run to the Data Merger. From there on the data can be handled like normal data. The SDAQ Supervisor is a program that handles the communication between COOR, the Data Merger and the various IOCs. EPICS is used for communication with the IOCs. The calibration result is

ultimately received from the Data Merger by the Calibration Manager which writes the data into the ORACLE database.

The operating system used on the IOC is VxWorks. VxWorks is a real time operating system that is supported by Fermilab. The SDAQ program running on the IOC can be split into two parts: the SDAQ Calibration and the SDAQ Monitororing system. During a calibration run the SMT readout receives triggers from the Trigger Framework. This ensures that triggers cannot occur while the SVX is reset and takes care of the synchronization between several readout crates and the synchronization of the SVX clock to the accelerator clock. A 64-bit DMA transfer is used to transfer the data from the VRBs to the IOC.

It is possible to examine the data while the data collection is ongoing. For this purpose a server process is running on the IOC which upon request sends out data to any client. Histoscope, a Fermilab histogramming package, is currently used to display the data. Data can also be transferred via EPICS.

The SDAQ program calculates pedestals, gains and their uncertainties for each of the channels at the end of a calibration run. The result is stored in the database. A separate process uses this information to calculate significant parameters for each readout chip: the threshold for zero suppression, the number of noisy strips, and the number of dead strips. Those results are stored in the database as well. The calculated threshold can be used as download parameter for the next data taking period.

The same SDAQ program is used for monitoring while a normal Primary Data Acquisition run is ongoing. In this mode the VRB transfers the data of one of its readout channels into a VRB internal Monitor FIFO. A prescale can be set to adjust the rate of monitor events. The 8KByte large FIFO can be read out either through the VME back plane or through an auxiliary port. The data is collected and analyzed by the IOC. Monitoring the occupancy allows a determination of when a new threshold needs to be found. Additional dead channels are determined as well. A message is sent to the Significant Event System if a parameter reaches a limit. Additionally summary information is written on a regular basis to the database. Upon request, complete histograms for specific channels are transferred to a client.

The offline monitoring is implemented with "Examine" processes, which allow one to fully reconstruct a small number of events. Apart from occupancy histograms this allows a SMT specific event display, Landau distributions of cluster charges and the reconstruction of tracks and vertices.

CHAPTER 9 - DETECTOR PERFORMANCE

9.1 Overview

The DØ Run 2B group performed a detailed simulation of the Run 2B silicon microstrip tracker. The simulation included a full Geant simulation of the underlying physical process, data-tuned models of detector response, and complete reconstruction of simulated events, including pattern recognition, within the DØ Run 2B software framework. Quantitative calculations of occupancy, impact parameter resolution, momentum resolution, and b-quark tagging efficiency verify substantial improvements in performance over the presently operating Run 2A silicon detector. These full Geant results are presented below.

In addition, qualitative "reality checks" were also performed using the Fermilab MCFAST package[1]. These studies were essential for iterating on geometries to optimize the design and comparing it to the Run 2A detector. MCFAST assumes perfect pattern recognition, and is most useful for studying resolutions and acceptances under varying conditions. We studied: occupancy, distance of closest neighboring hits, efficiency of reconstructing B-hadron decays, impact parameter resolution, vertex resolution, and decay length significance. In addition, with another toy MC model we optimized the ganging of sensors for staves. A summary of the results for the distance of closest neighboring hits is presented here and the detailed discussion of these results is found in DØnote-3911.

For logistical reasons, the layout used for the Geant simulation was frozen in August 2001. The minor differences between simulated layout and TDR baseline design are summarized in the next section.

9.2 Silicon Geometry In The Simulation

The Run 2B silicon detector is modeled as a barrel tracker consisting of six concentric cylindrical layers, numbered from 0 to 5 in going from the innermost radius of 19 mm to the outermost radius of 164 mm, respectively. Pseudorapidity coverage extends from -2.5 to +2.5. Each layer consists of two sub-layers that preserve a six-fold symmetry for the silicon track trigger. Layers 0 and 1 were simulated with axial silicon detectors only, while layers 2 through 5 contained axial-stereo pairs of single-sided detectors in each sub-layer. Figure 73 shows an *x-y* view of the Run 2B silicon detector geometry as implemented in the simulations; and Table 10 gives positions, dimensions, and stereo angles of the detector modules used for this work.

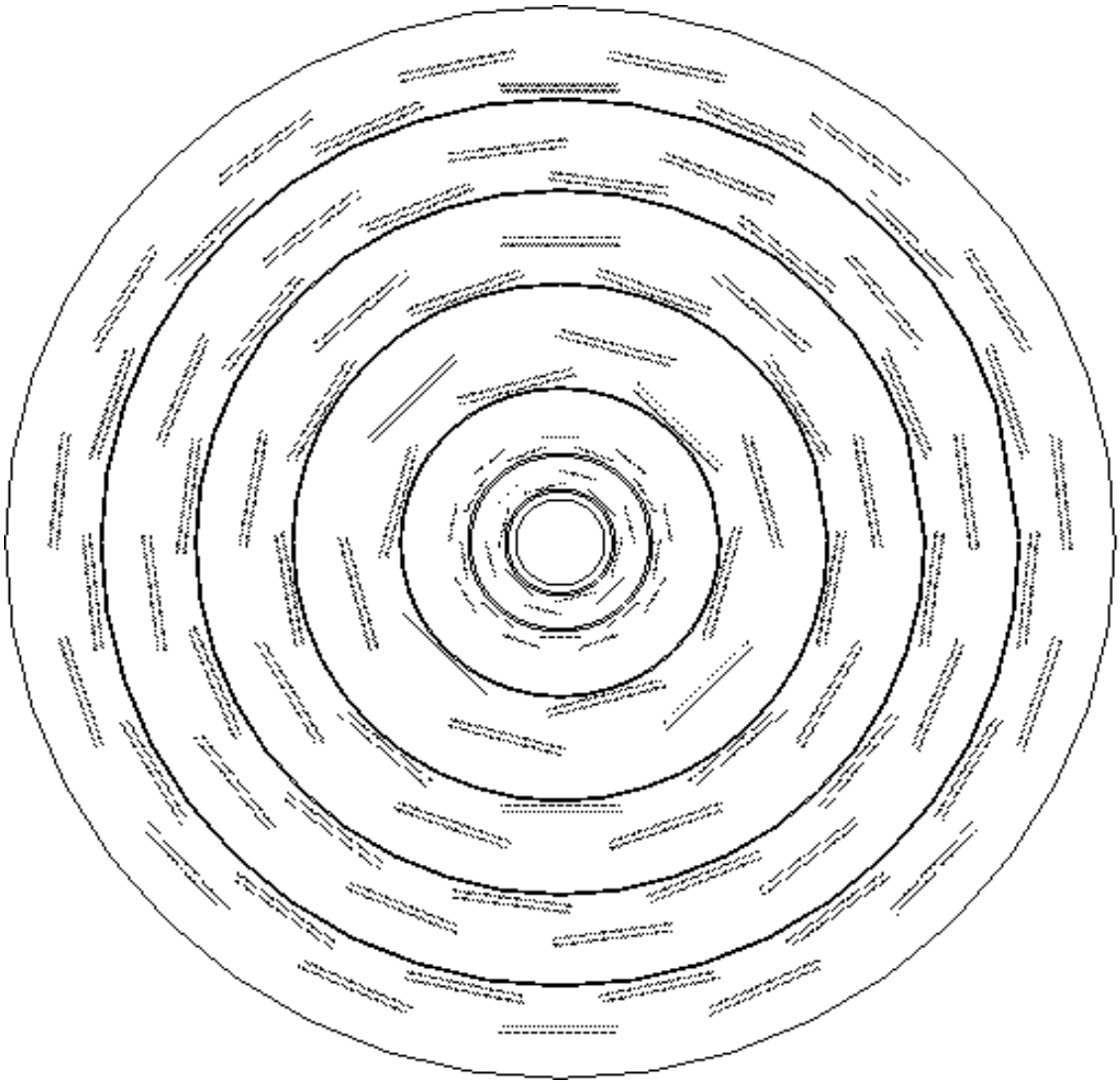


Figure 73 - Geometric layout used in Geant simulation of Run 2B silicon detector.

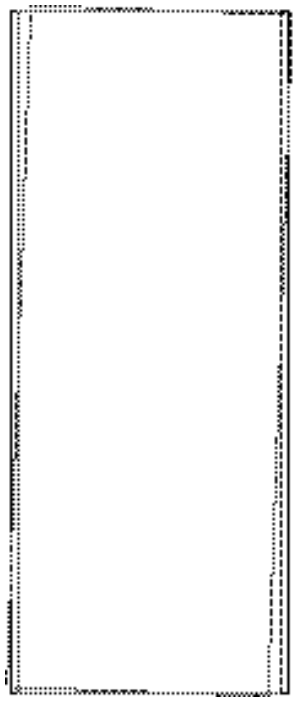


Figure 74 - Layout of an axial-stereo module.

Barrel modules are assembled end-to-end on long staves placed on carbon fiber support cylinders that lie parallel to the *z*-axis of the detector. Staves hold five modules each in layers 0-3 and six modules in layers 4-5. The design of the Run 2B silicon detector requires axial modules and two kinds of axial-stereo "sandwiches". The axial type is simulated as a silicon plate of 1.48 cm width, 7.84 cm length and 300 μm thickness. A sandwich silicon module consists of two equivalent silicon sensors, one axially oriented and the other rotated with respect to the beam axis. The radial distance between the two silicon planes in the sandwich is 2.3 mm, and the angle of the rotation is ±2 degrees. The size of the silicon ladders in the sandwiches is 5 cm × 10 cm × 300 μm. An *x*-*z* view of a +2 degree version is shown in Figure 74.

Low mass readout cables are modeled as copper plates of 1 cm width that go out of the edge of first and third silicon modules in every layer.

Table 10 - Parameters of the Run 2B silicon tracker used in the GEANT simulation.

Layer	***Radius (cm)***	***# of sensors in z***	***Sensor Length (cm)***	***Sensor Pitch (mm)***	***Stereo angle (degrees)***
0a, 0b	1.90 / 2.34	10	7.84	50	0 / 0
1a, 1b	3.17 / 3.54	10	7.84	50	0 / 0
2a, 2b	5.42 / 6.77	10	10.0	60	-2 / +2
3a, 3b	8.93 / 10.11	10	10.0	60	-2 / +2
4a, 4b	12.15 / 13.26	12	10.0	60	-2 / +2
5a, 5b	15.24 / 16.32	12	10.0	60	-2 / +2

The main difference between the simulated layout and TDR baseline Run 2B silicon detector design is in the number of sensors along the beam in layers 0 and 1. This leads to an underestimate of the $|\eta|$ coverage compared to what should be achievable in Run 2B. The TDR mechanical design also implements multiple stereo angles for the silicon detectors assembled into the modules: 2.5^o for $|z|<30$ cm and 1.25^o at $|z|>30$ cm. Other differences also include a different readout pitch for layer 1 which is simulated with 50 μm pitch as opposed to the 58 μm pitch for the baseline design. No major differences are expected between results from the simulation and those to be achieved in the final design; this is now being checked with a more refined detector model.

9.3 Simulation Of Signal, Digitization And Cluster Reconstruction

Geant simulates hits in the silicon sensors, and a modified DØ Run 2A package DØSim[2] package digitizes signals. Input for DØSim consists of a bank of GEANT hits, each of which is described by entry/exit positions and energy deposition in the silicon. Silicon *dE/dx* is simulated via explicit generation of δ-rays that resulted in a Landau distribution of deposited energy. No additional fluctuations in energy loss were considered.

The total deposited energy is converted into the number of electron-hole pairs using a coefficient $C=2.778\times10^8$ GeV^{-1}. Charge collection on strips is computed from a diffusion model with the standard drift and Hall mobility of the charge carriers in silicon evaluated at the nominal silicon operating temperature. Charge sharing between strips through intermediate strip wiring is determined by inter-strip capacitance, readout-ground capacitance, and the input capacitance of preamplifier, values of which are taken from Run 2A measurements.

Electronic noise is added to the readout strips after hits have been digitized. Parameters for noise simulation were extracted from the readout electronics noise parameterization and silicon detector prototype studies for Run 2A[3]. This set of parameters leads to a S/N ratio of 16:1, and this value is used for all tracking performance studies. For occupancy studies the average noise was simulated for each channel according to Gaussian distribution with $\sigma=2.1$ ADC counts that decreases the signal-to-noise ratio to 10:1, again consistent with the Run 2A data. A similar signal-to-noise ratio is expected for the end of Run 2B (see the section on sensors). Only those strips above a threshold of 4 ADC counts are saved for cluster reconstruction.

The choice of the threshold for the readout and cluster reconstruction represents a trade-off between efficiency of the cluster reconstruction and noise suppression. Figure 75 shows the probability to read out a strip as a function of strip energy deposition in minimum ionizing particle (MIP) equivalents, and to have a fake hit due to electronic noise as function of the readout threshold. One can see that a readout threshold of 6 ADC counts leads to 20% probability of losing a strip that collects 1/3 MIP while significantly suppressing the noise contribution.

Reconstruction of one-dimensional clusters was performed using a modified package for Run 2A cluster finding. The clusters are defined as a collection of neighbor strips with total charge more than 12 ADC counts. Only those strips registering above 6 ADC counts are allowed in the

cluster. The position of the cluster is calculated with a center of mass algorithm independent of the cluster size.

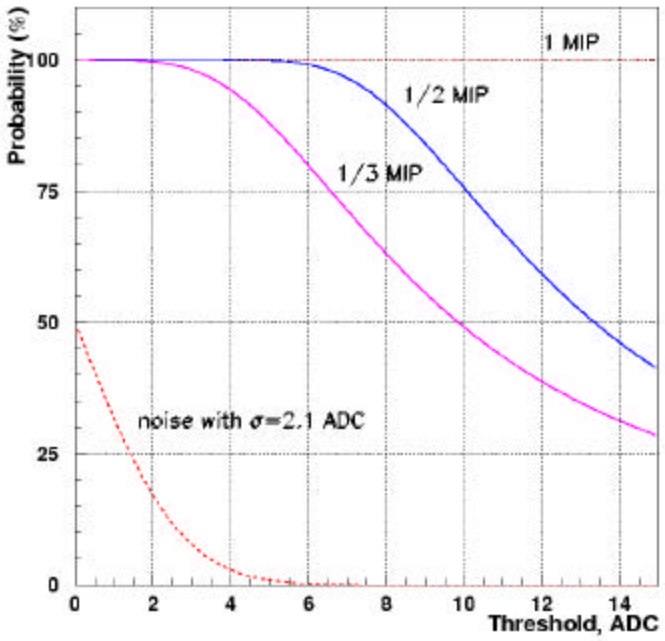


Figure 75 - Probability to have a hit on strip with different fraction of MIP's charge.

9.4 Analysis Tools

Occupancy and position resolution studies utilize a modified Run 2A DØ SmtAnalyze package that allows access to raw and digitized Geant hits and reconstructed clusters. Pattern recognition was performed using the DØ Run 2A Histogramming Track Finder[4] (HTF) modified for Run 2B-specific geometric features. The HTF algorithm is based on pre-selection of hit patterns ("templates") in both the silicon detector and the DØ fiber tracker with particular r-ϕ and z-η properties. Hit patterns are further cleaned and fitted using a standard Kalman filtering technique. The separation of r-ϕ and stereo measuring detectors in the Run 2B silicon detector by a finite gap required modification to HTF as the precise z position of hits could be determined only after the actual track direction was found. After suitable adjustment, HTF demonstrated the good performance seen for Run 2A. All results assume no degradation in fiber tracker performance between Run 2A and Run 2B.

9.5 Performance Benchmarks

Basic tracker performance was studied with 2000 event single muon samples generated with transverse momenta of 1, 5, and 50 GeV/c. The primary vertex was fixed in the transverse plane at x=y=0; and z was distributed about zero with a 15 cm Gaussian width.

For estimation of the physics performance, representative signal channels have been chosen and simulated with zero or six minimum bias (MB) events overlayed. Pattern recognition, track reconstruction in jets, and b-tagging efficiency were studied by examining associated production of Higgs with a W-boson. The Higgs boson mass was chosen to be 120 GeV/c^2, and the Higgs was forced to decay to a bb pair. Z-boson production followed by decay to light quarks was used to estimate the fake rate of the b-tagging algorithm. Minimum bias events were generated with PYTHIA using a set of parameters tuned to CDF run 1 minimum bias data[5]. Samples of at least 2000 events were processed through the full simulation chain for all studies, with larger samples of 5000 events used for luminosity and occupancy studies.

9.6 Results

9.6.1 Occupancy

Occupancy in the innermost layers is one of the most important issues for the Run 2B silicon detector operation and performance. Four concerns related to occupancy impact the design. The first, radiation damage limits the lifetime of the sensors and its dependence on radius, is discussed in detail in the section devoted to sensors. Second is the number of hits per module to be read out per event, which can cause excessive dead time if too large. The relationship between number of hits and charge collection per strip is addressed in the electronics section. The other concern is that a high occupancy in the innermost layer might lead to a significant fraction of wide clusters formed by overlapping tracks that may worsen spatial resolution. The occupancy is also an important factor in the pattern recognition.

Occupancy has been studied in detail using the samples of WH events both with and without six additional minimum bias events, and with pure minimum bias events. In all cases, electronic noise was added to physics events. Minimum bias events were used to estimate the average occupancy as a function of radius. Peak occupancies occur in the WH with six superimposed minimum bias events and were estimated by looking at the silicon module with the highest number of fired strips. The highest local occupancy occurs within a jet. If this value is too high, both pattern recognition and impact parameter performance will be degraded, resulting in a loss of b-tagging efficiency and consequent physics reach.

Average occupancy in minimum bias events with and without noise as a function of radius is shown in Figure 76. The plot clearly demonstrates that the average occupancy due to physics processes in minimum bias events is of about an order of magnitude less than that due to noise in the system. The occupancy caused by hits from real particles drops with radius as expected, and the noise occupancy practically does not change with radius. This behavior is in part due to the relatively low threshold used for the study.

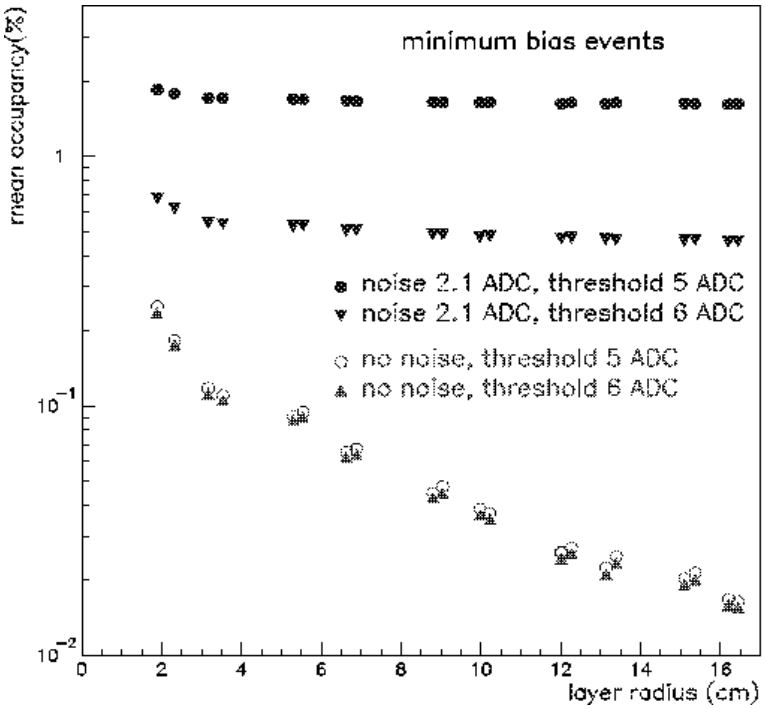


Figure 76 - Mean occupancy as function of radius in minimum bias events without noise and with average noise.

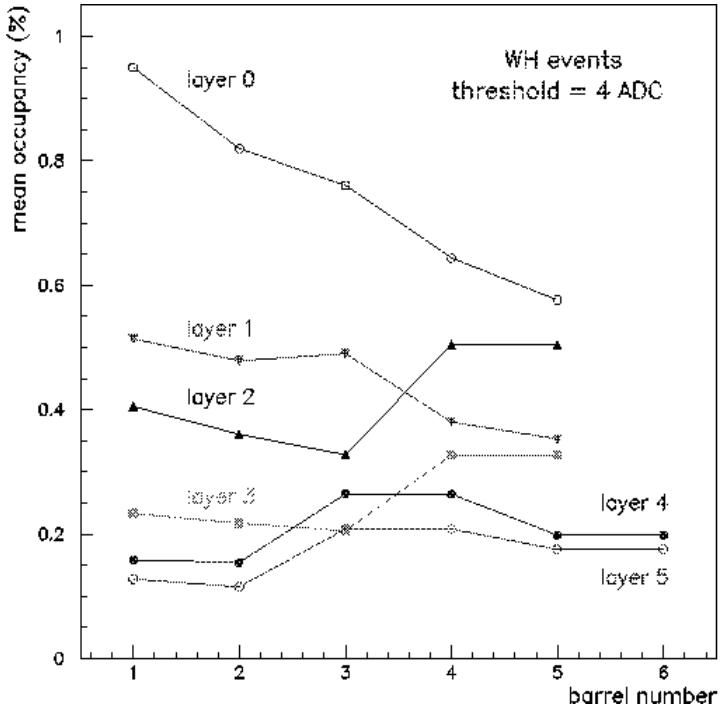


Figure 77 Mean occupancy as function of z-position of a silicon module at different radii. Higher barrel number corresponds to higher z values.

Figure 77 represents the z-dependence of the average occupancy for WH events without noise in the system. It decreases by 50% for layer 0 away from *z=0*. At large *z*, two silicon modules in layers 2 through 5 are bonded to each other ("ganged") to minimize cable count. Occupancy for these layers clearly increases in the outer barrels where ganging is applied, but not to a level that harms detector performance.

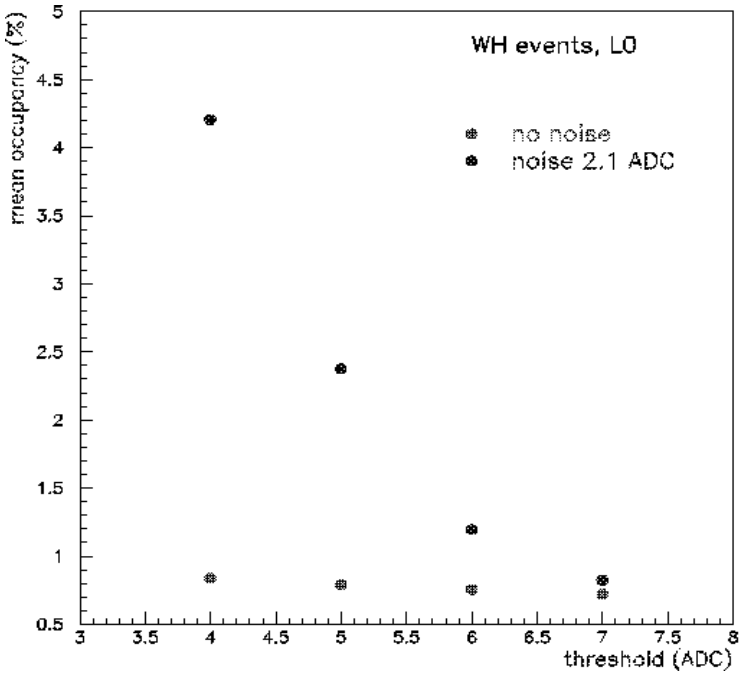


Figure 78 - Mean occupancy in layer 0 without noise and with average noise as a function of the readout threshold.

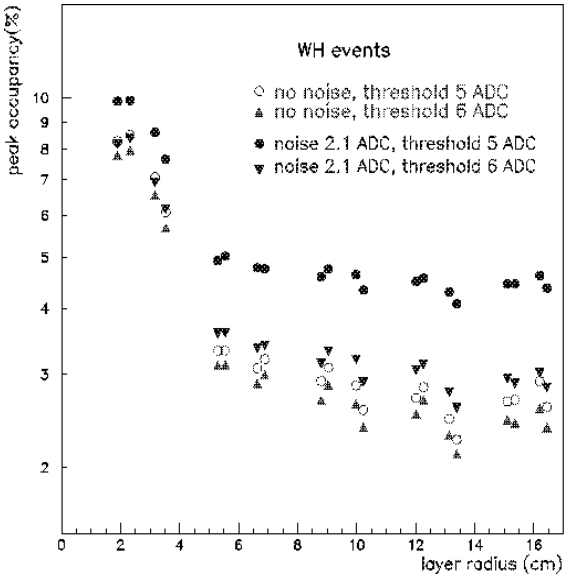


Figure 79 Peak occupancy without noise and with average noise at different readout thresholds as function of the radius.

Dependence of the average occupancy on the readout threshold is shown in Figure 78 for WH events without pile-up. A reduction factor of 1.8 in the average occupancy can be obtained by using a threshold of 5 ADC counts. An additional reduction factor of two can be achieved by using the readout threshold of 6 ADC counts. This does not significantly affect the signal readout efficiency while the S/N ratio is higher than 10:1; but losses of efficiency would be expected for smaller S/N ratios.

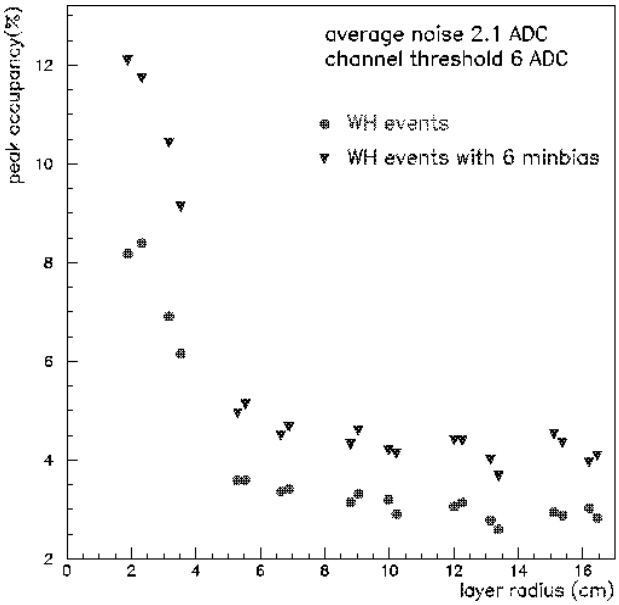


Figure 80 - Peak occupancy in WH events without pile-up and with 6 minimum bias events as function of the radius.

Peak occupancy as a function of radius for b-jets in WH+0 MB events is shown in Figure 79. At small radii (less than 5 cm), peak occupancy drops from 8% in layer 0 to 6% in layer 1b. For larger radii occupancy is nearly independent of radius since the size of the b-jet is smaller than the area of a module. Dependence of the peak occupancy on luminosity is shown in Figure 80. At the higher luminosities corresponding to an additional 6 MB events peak occupancy increases by a factor 1.5 in all layers compared to low luminosity case.

9.6.2 Cluster size and spatial resolution

Spatial resolution plays an important role in the impact parameter resolution and in pattern recognition. Factors determining spatial resolution include detector pitch, presence of intermediate strips, signal-to-noise ratio, the clustering algorithm, Lorentz angle, and direction of the track.

The importance of two-track resolution in reconstructing b-quarks jets can be immediately appreciated from Figure 81. The results shown in this figure have been obtained using the MCFAST simulation referred to above. This figure shows the fraction of tracks from B-decays in WH events which have a nearest neighboring hit within a given distance as a function of radius near z = 0.0 cm. The neighboring hit can be from any other track. The plot is taken from a sample of events with no extra minimum bias events. Adding in five minimum bias events did

not change the plot, showing that close neighboring hits arise from within the B-jet itself. Fractions for three different distance windows are shown. At the smallest radius (2.0 cm), more than 50% of the tracks have nearest neighbors within 300 microns.

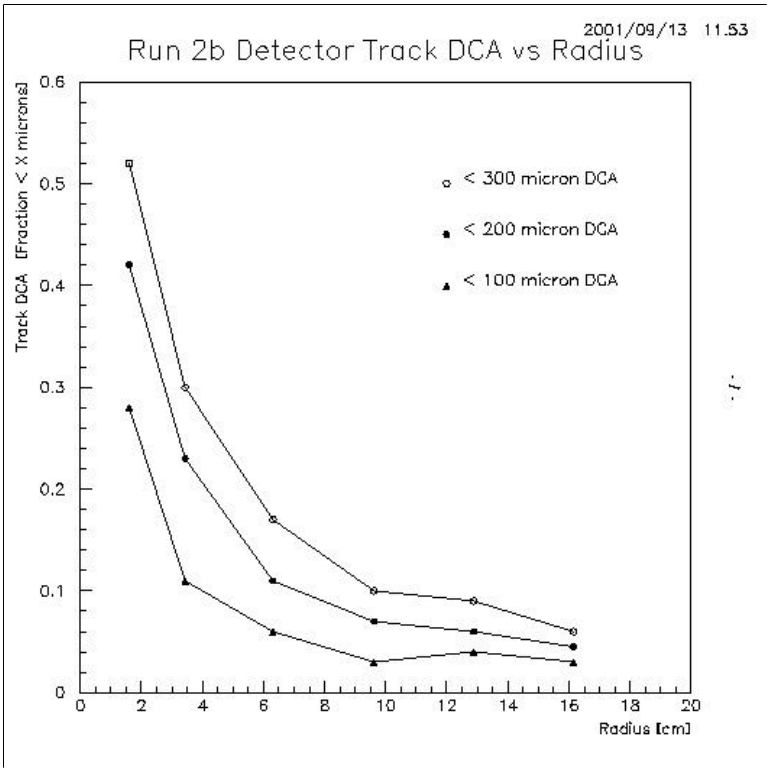


Figure 81 - Fraction of tracks that have a nearest neighboring hit within a given distance as a function of radius near z = 0.0 cm, for three different distance windows.

The two inner layers are equipped with 50 μm pitch sensors, and the outer four layers contain sensors with 60 μm pitch. Figure 82 shows the fraction of clusters as a function of number of strips for single muons in the inner and outer layers. Intermediate strips cause two-strip clusters to dominate, leading to an intrinsic single cluster resolution of about 6 μm. Fractions of one-, two- and three-strip clusters are shown in Table 11 together with expected spatial resolutions. Resolutions derived from one- and three-strip clusters are given in Figure 83 and Figure 84, and are approximately the same for inner and outer layers. No mis-alignment of the silicon detectors was assumed.

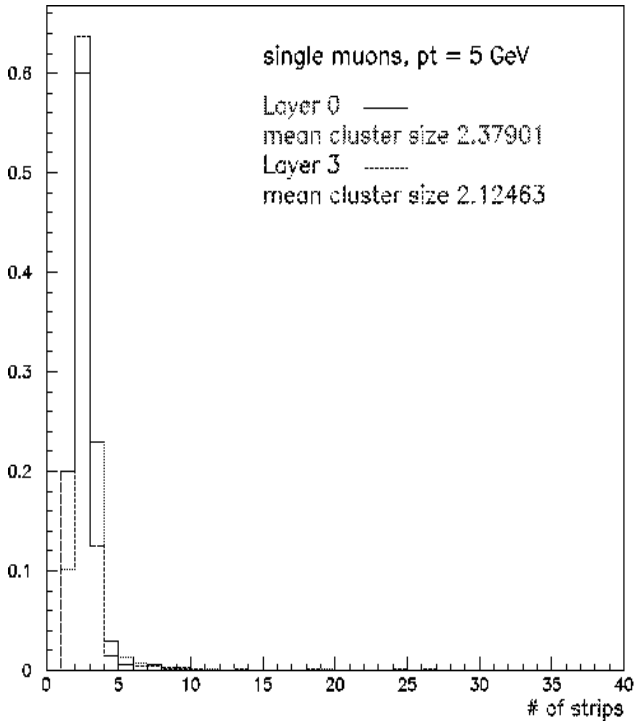


Figure 82 - Cluster size distribution in layer 0 with 50µm readout pitch and layer 3 with 60µm readout pitch.

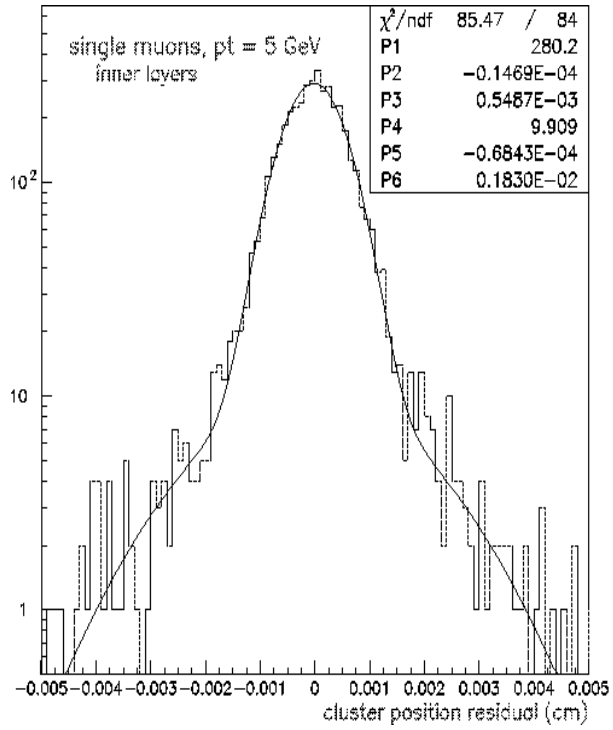


Figure 83 - Spatial resolution derived from the clusters in the two innermost layers with readout pitch of 50 µm.

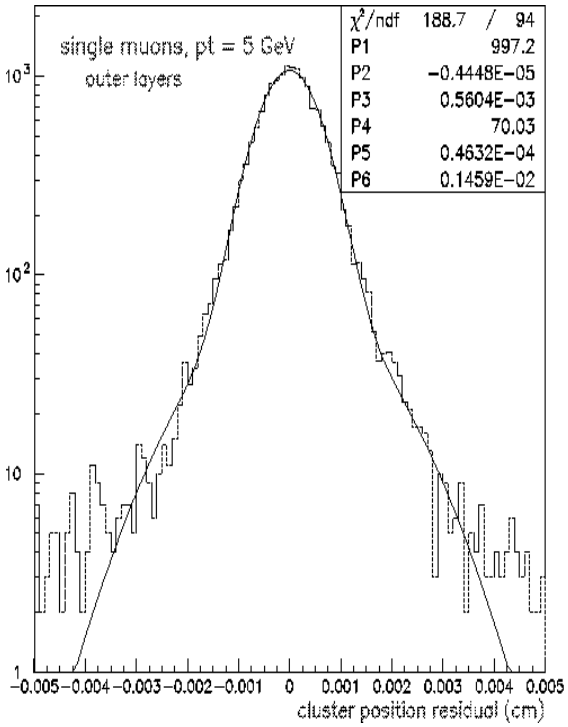


Figure 84 - Spatial resolution derived from the clusters from four outer layers with readout pitch of 60 µm.

Table 11 - Position resolutions for various cluster sizes.

	Layers 0,1			**Layer 2-5**		
Number of strips	1	2	3	1	2	3
Fraction of clusters	0.1	0.6	0.23	0.2	0.64	0.13
Resolution (μm)	6.8	5.3	6.7	8.2	5.5	8.1

Figure 85 and Figure 86 show distributions of the number of strips in clusters for WH and WH events with pile-up. The average number of strips per cluster for physics events is higher than for single muons.

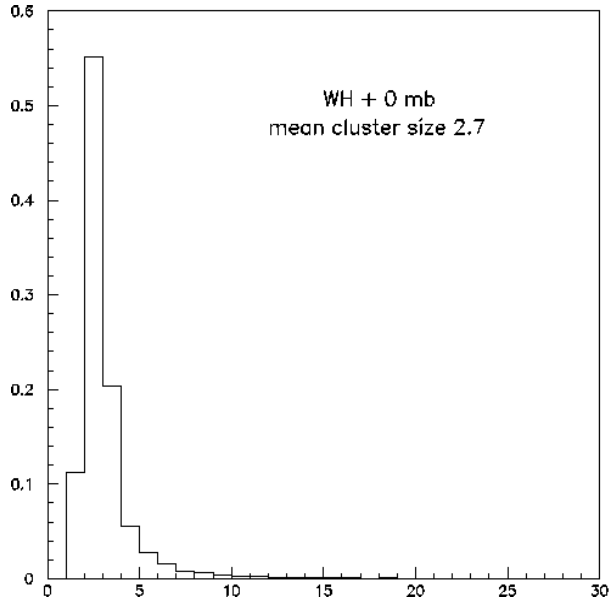


Figure 85 - Cluster size (number of strips) in WH events without pile-up.

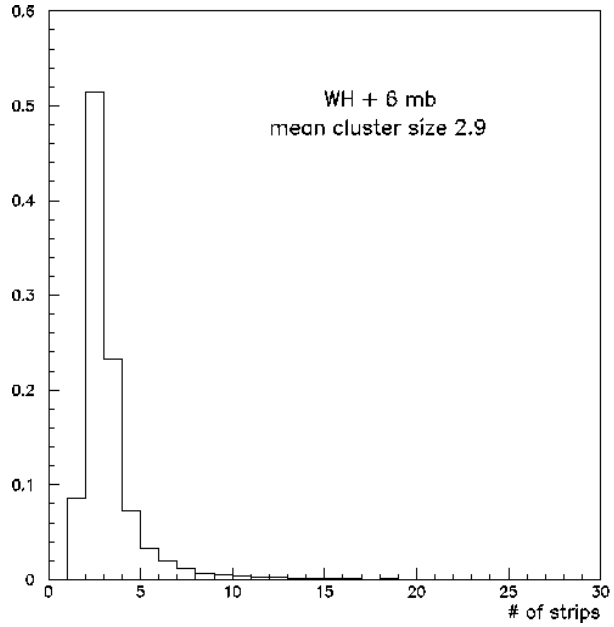


Figure 86 - Cluster size (number of strips) in WH events with an additional 6 minimum bias events.

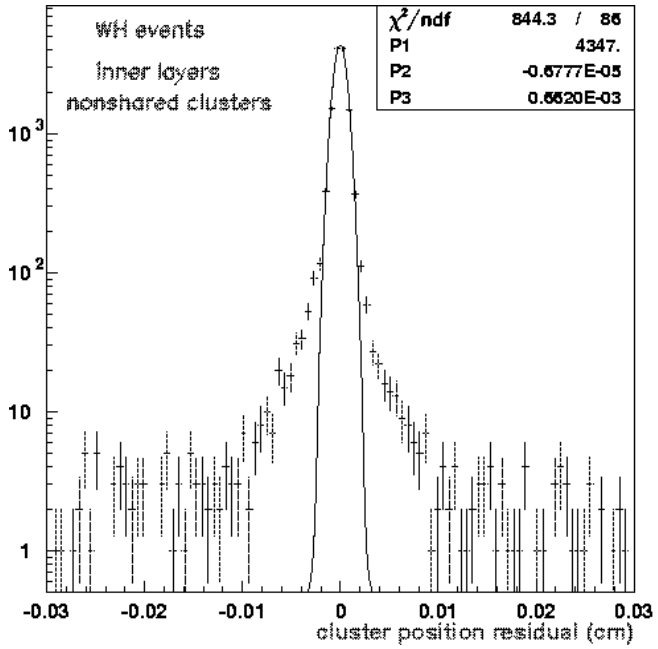


Figure 87 - Hit position resolution in WH events obtained with non-shared clusters.

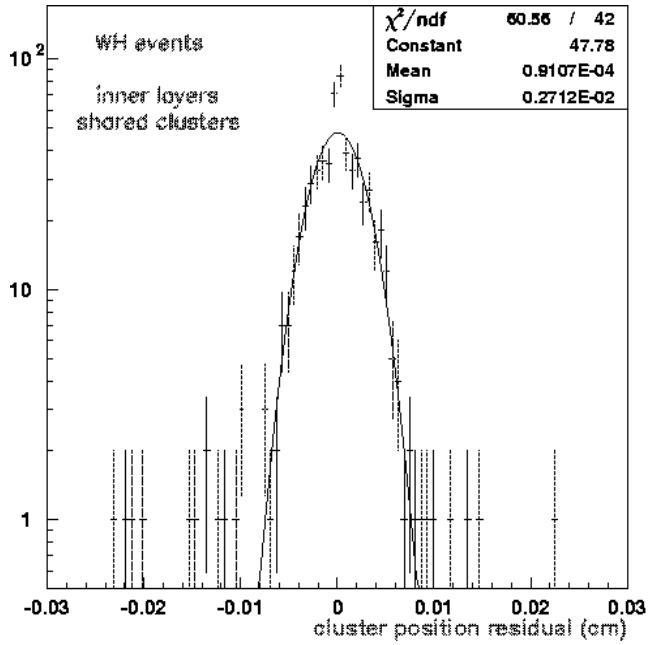


Figure 88 - Hit position resolution in WH events obtained with shared clusters.

Clusters formed by more than one track are denoted as "shared clusters". Cluster sharing leads to worse spatial resolution, reduced ability to find tracks close together, and a drop of impact parameter resolution and b-tagging efficiency in the end. The spatial resolution for clusters produced by one track is about 7 μm (Figure 87) while the hit position resolution in the inner layers for WH events for shared clusters is about 27 μm (Figure 88). Figure 89 shows the probability for N tracks to share a reconstructed cluster as a function of N. One can see that this distribution is wide, and the fraction of multi-track clusters formed by more than two tracks is about 90%. The average number of tracks in shared clusters is 6.5, leading to the observed serious degradation of spatial resolution for these cases. Another way of saying this is that the peak at small track separation evident in Figure 89 is due to having many tracks close together in a relatively small number of events. This high multi-track correlation effect does not easily reveal itself in simple parametric Monte Carlo studies performed with tools such as MCFast.

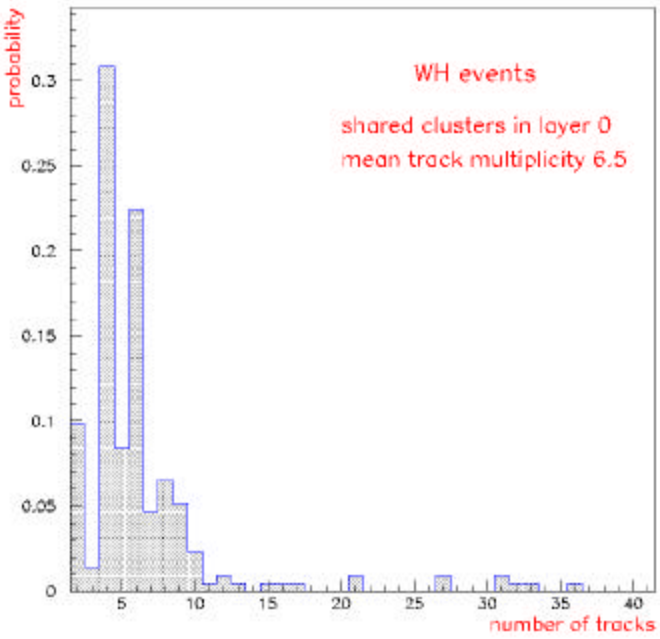


Figure 89 - Average multiplicity of the tracks which form a shared cluster.

The fraction of shared clusters is shown in Table 12 for WH and WH events with pile-up for different layers. The largest cluster sharing of about 6% is observed in layer 0. The fraction of shared clusters decreases with radius for the inner layers and is almost constant for the outer ones since the separation of tracks in b-jets increases modestly over the silicon detector volume.

Table 12 - Percentage of shared clusters vs. layer for WH events with and without six minimum bias events overlaid.

	L0a	**L0b**	**L1a**	**L1b**	**L2a**	**L2b**	**L3a**	**L3b**	**L4a**	**L4b**	**L5a**	**L5b**
WH events	5.3	4.5	3.5	3.0	2.3	2.2	1.3	1.4	1.1	0.96	0.9	1.0
WH with 6 minimum bias	5.9	4.7	3.5	3.2	2.5	2.1	1.5	1.4	1.1	1.0	0.9	1.0

9.7 Physics Performance Of The Run 2B Tracker

As discussed earlier in this document, the main Run 2B physics goal is the search for the Higgs boson. Other important investigations will center on top-quark properties, precision measurements of W-boson mass and width, b-physics, and searches for supersymmetry and other new phenomena. All physics would benefit from improved track reconstruction efficiency and momentum resolution in a Run 2B tracker with an upgraded silicon detector. However, higher b-tagging efficiency keys new physics discovery potential in DØ.

The following sections summarize the track reconstruction efficiency, accuracy of the track parameter measurements, and b-tagging efficiency obtained from studies of WH events.

9.7.1 Single track performance

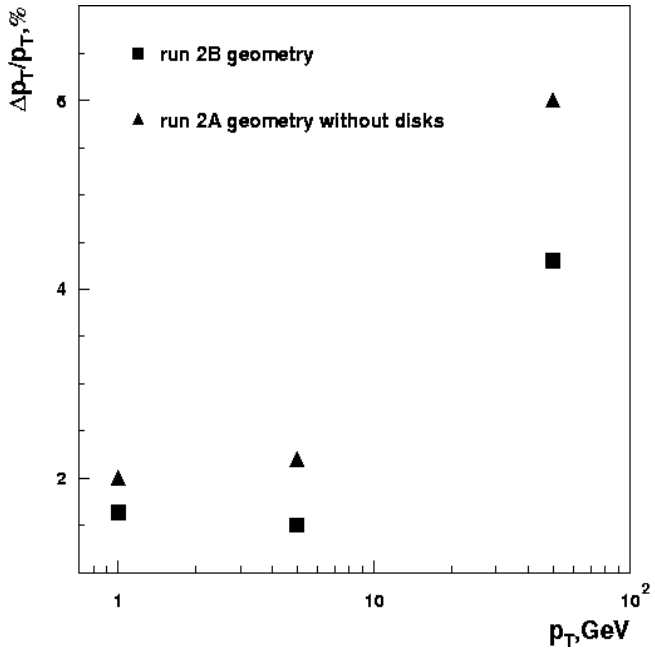


Figure 90 - pT-resolution as a function of pT for single muons in Run 2A (without disks) and Run 2B.

The p_T resolution $\sigma(p_T)$ for single muons is shown in Figure 90, together with $\sigma(p_T)$ calculated for the Run 2A tracker. In order to make the two geometries more similar and thus provide more consistent comparison in the forward $|\eta|$-region, the F- and H-disks were taken out of the Run 2A simulation. The resolution in Run 2B is expected to be 1.5 times better than the existing tracker. The main reason for that improvement is the larger number of precision measurements per track, particularly at larger $|\eta|$.

Reconstruction efficiency as function of $|\eta|$ is shown in Figure 91. It is fairly flat up to $|\eta|=1.5$ for all transverse momenta. Because tracks at larger η miss the fiber tracker altogether and cannot produce the minimum four hits required for silicon-only tracking, the reconstruction efficiency begins dropping above $|\eta|=1.5$, falling to 90% by $|\eta|=2$.

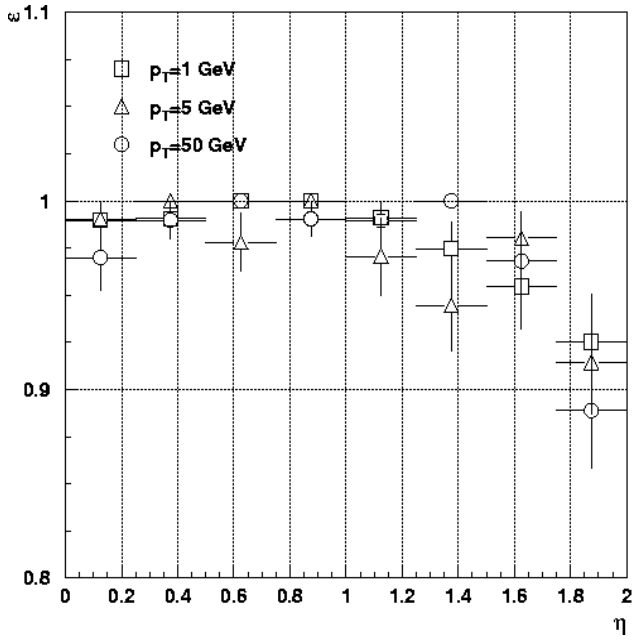


Figure 91 - Reconstruction efficiency as function of ? of muons with pT=1,5,and 50 GeV/c.

Impact parameter resolutions in the transverse plane and *z*-direction are important for heavy-flavor tagging, primary vertex reconstruction (especially at high luminosity), and detection of secondary vertices. At high momenta (p_T>10 GeV), resolution is determined to a large extent by the measurements in layer 0. At smaller momenta, it depends on multiple scattering and therefore the material distribution in the tracker. Transverse impact parameter resolution as function of p_T of single muons is compared to that in Run 2A in Figure 92. Improvement by a factor of 1.5 is expected for $\sigma(d_0)$ over the whole p_T region. This can be understood as being due to the closer (to the interaction point) first measurement in the Run 2B silicon detector and to the larger number of precision measurements. Indeed, for a simple two layer detector with measurements of hit resolution σ_{meas} at radii R_{inner} and R_{outer}, the impact parameter resolution is simply $\sigma(d_0) \sim \sigma_{meas}(1+R_{inner}/R_{outer})$. The ratio R_{inner}/R_{outer} is 0.27 in Run 2A and 0.11 in Run 2B. This geometric change accounts for almost all of the impact parameter resolution improvement.

The transverse impact parameter resolution $\sigma(d_0)$ as function of $|\eta|$ is shown in Figure 93 for the Run 2B tracker and for the Run 2A tracker without disks. For Run 2B, a slight degradation in $\sigma(d_0)$ is observed for low-p_T tracks with increasing $|\eta|$; for high-p_T tracks the distribution of transverse parameter resolution vs. $|\eta|$ is flat. These behaviors are expected from the enhanced contribution of multiple scattering at large $|\eta|$ and small p_T

Dependence of the longitudinal impact parameter resolution on p_T is shown in Figure 94. Because of the absence of three-dimensional measurements in layer 0 and the relatively worsened *z*-resolution obtained with 2^o stereo detectors compared to the 90^o detectors in Run 2A, the resolution in longitudinal impact parameter resolution in Run 2A degrades to 280 μm for high-p_t muons.

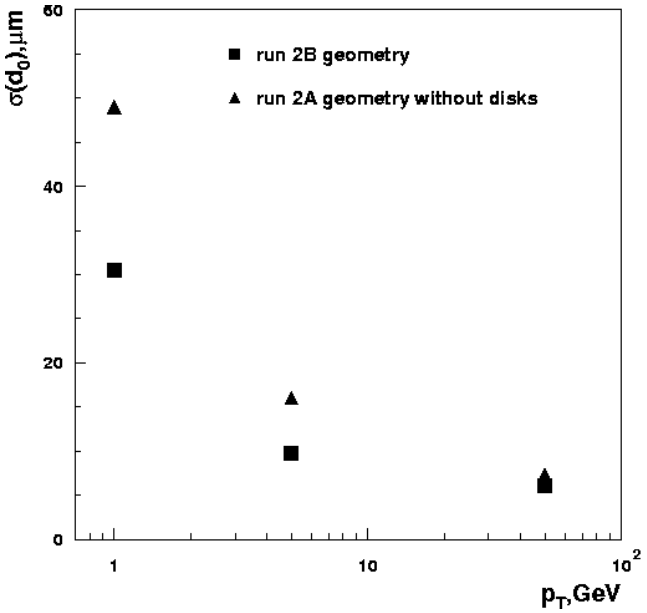


Figure 92 - Transverse impact parameter resolution as function of pT for single muons.

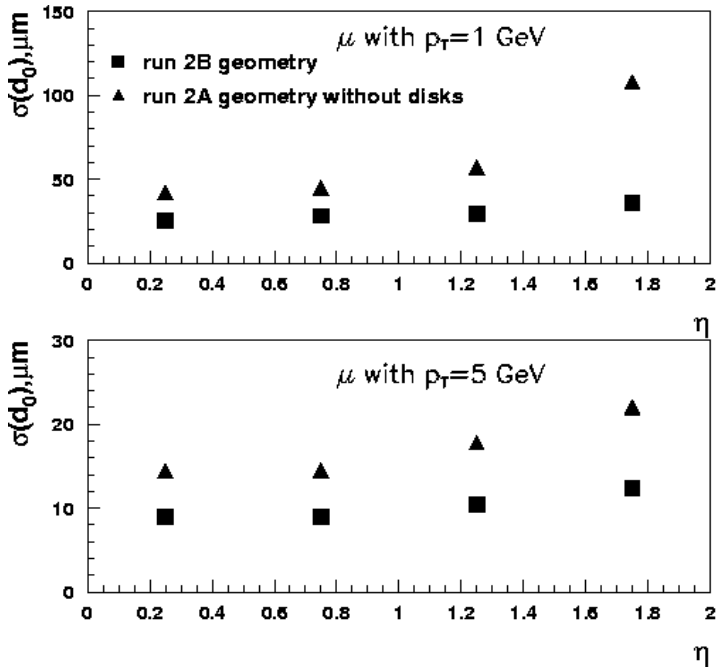


Figure 93 - Comparison of the transverse impact parameter resolutions in Run 2A and Run 2B for low-pT muons.

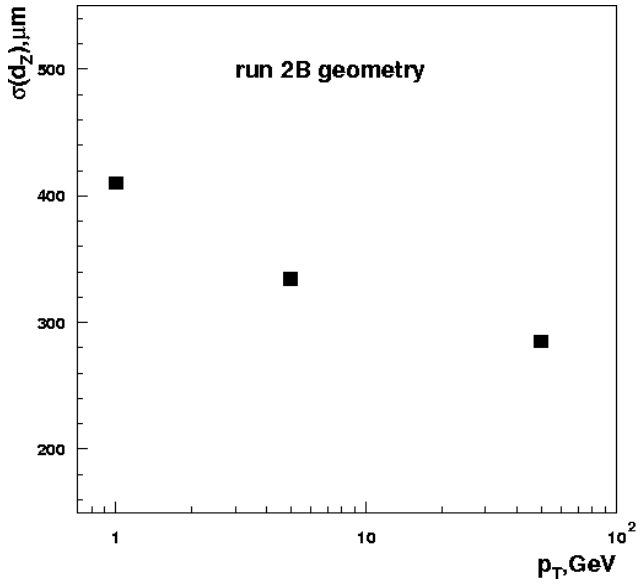


Figure 94 - Longitudinal impact parameter resolution as a function of pT for single muons.

9.7.2 b-tagging performance

B-tagging is the main tool for searches for the Higgs boson and many supersymmetric objects, as well as for top physics. The main goal of b-tagging methods is to reject jets produced by light quarks and gluon jets while preserving a high efficiency for tagging of the b-jets. Pre-selection of b-jets is based on the relatively long lifetime of B hadrons. Rejection of charm jets is limited by the finite lifetime of charmed hadrons, and rejection of gluon jets is bounded by contributions from gluon splitting to heavy quarks at branching fractions of a few percent. Experimental limitations for ideal b-tagging arise from inefficiencies of the track reconstruction in jets, impact parameter resolution and secondary vertex resolution.

The overall track reconstruction efficiency in jets together with the corresponding fake track rate is presented in Table 13 for WH events at low and high luminosities. There is slight degradation in the track finding efficiency at high luminosity, but the fake track rate is negligible in both cases. The average track reconstruction efficiency in jets $\varepsilon_{tr\text{-}j}$ is consistent with that for Run 2A.

Table 13 - Track reconstruction efficiency and fake track rate in jets in WH events without pile-up and with 6 minimum bias events.

	$e_{tr\text{-}j}$	***Fake rate***
WH + 0 min bias events	84%	0.0%
WH + 6 min bias events	81%	0.1%

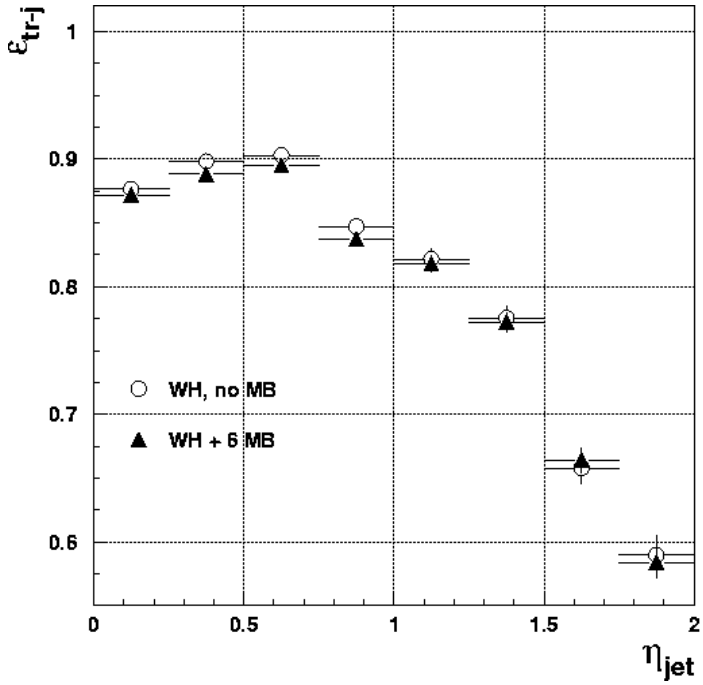


Figure 95 - Track reconstruction efficiency in b-jets as function of the |?| of the jet.

Figure 95 shows ε_{tr-j} as function of the jet $|\eta|$ for WH+0MB and WH+6MB events. The behavior of ε_{tr-j} in jets is similar to the single-track performance. It is high (~88%) in the central region and quickly degrades beyond the fiber tracker boundary to ~60% at $|\eta|$=2. The relative drop in efficiency for higher $|\eta|$ is more pronounced in jets than observed for isolated muons. That can be explained by the fact that the more energetic jets at higher $|\eta|$ produce higher track multiplicity, making pattern recognition more complicated. Taking into account that b-quarks from Higgs boson decays and top decays produce mostly central jets, one can expect the overall performance to be dominated by a track reconstruction efficiency in jets of 85-88%.

A signed impact parameter (SIPtag) method[6] was used to evaluate b-tagging performance. A SIPtag requires that:

- Tracks lie within a cone $\Delta R < 0.5$ around the jet axis;
- Selected tracks have $p_T > 0.5$ GeV/*c*, good reconstruction quality, and at least two hits in the silicon;
- At least two tracks have an impact parameter significance $S = d_0/\sigma(d_0) > 3$ or at least three tracks have $S > 2$.

To estimate the "true" b-tagging efficiency the numbers of b, c, and s and light quarks with E>20 GeV and $|\eta| < 2$ were counted; and their parameters were compared to those of tagged b-jets. If a tagged jet was within a cone distance $\Delta R < 0.5$ about one of the light quarks, the flavor of that quark was assigned to the jet.

The b-tagging efficiency ε_b is defined as the ratio of the number of jets with assigned b-flavor to the total number of b-quarks in the considered acceptance. The mistagging rate is defined as the ratio of the number of b-tagged jets originating from light quarks to the total number of jets produced by light quarks in the considered $(E,\eta)_{jet}$ acceptance.

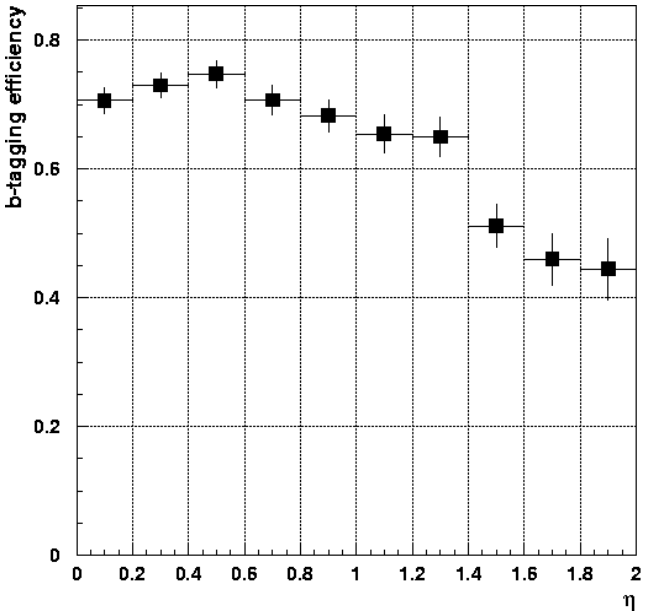


Figure 96 - b-tagging efficiency as function of |?| of the tagged jet.

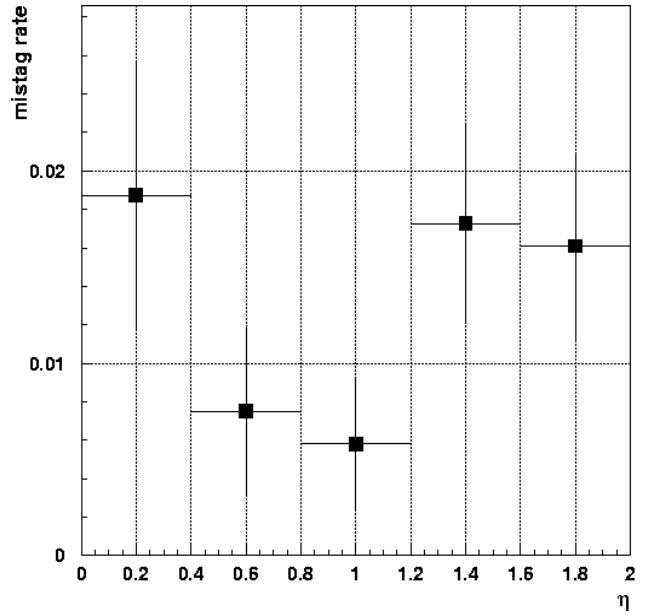


Figure 97 - Mis-tagging rate as function of |?| of the tagged jet.

Figure 96 shows the b-tagging efficiency ε_b vs. $|\eta|$ of the reconstructed b-jets in WH +0 MB events. The average ε_b per jet of 69% is 19% higher than in Run 2A. This is a consequence of

the improved impact parameter resolution due to the presence of layer 0. The b-tagging efficiency is above 70% for $|\eta|<1$, reflecting the high track reconstruction efficiency in jets in that region. It decreases with increasing $|\eta|$ to 45% at $|\eta|=2$. Dependence of the mis-tagging rate on the jet $|\eta|$ was studied using Z-boson decays to light quarks; it is shown in Figure 97. The mis-tagging rate varies between 1% and 2% over the whole $|\eta|$ region. This is roughly two times better than the expected Run 2A performance.

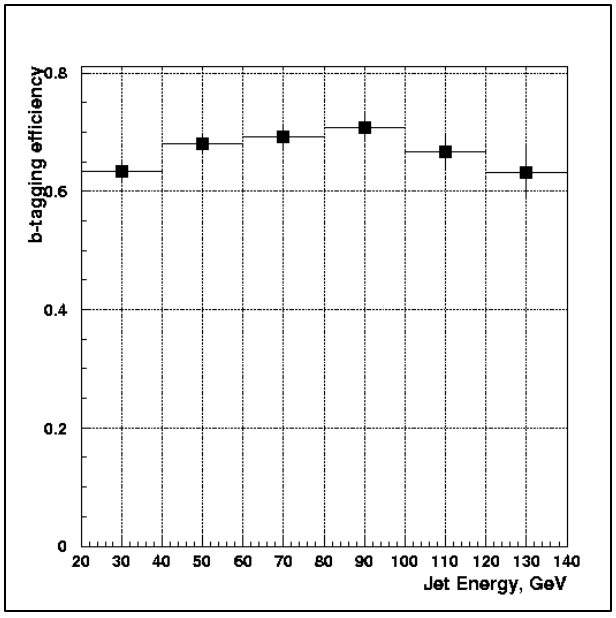


Figure 98 - b-tagging efficiency as function of the energy of the tagged jet.

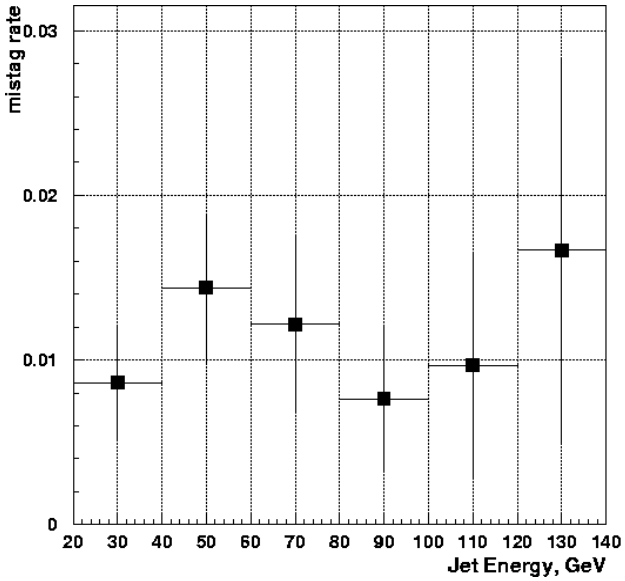


Figure 99 - Mis-tagging rate as function of the energy of the tagged jet.

Dependencies of the b-tagging efficiency and the mis-tagging rate on reconstructed jet energy E_j are shown in Figure 98 and Figure 99, respectively. The best performance in terms of b-tagging is expected for jets with E_j ~ 70-100 GeV. The rise of efficiency above 150 GeV is not statistically significant. Due to insufficient statistics, the mistagging rate is estimated only up to 140 GeV and is demonstrated to be about 1.5 % in the whole considered energy scale.

Probabilities to tag an event with one or two b-jets are shown for Run 2A (estimated from Z-boson decays to bb) and Run 2B (from WH events) in Table 14.

Table 14 - Probabilities to tag an event with one or two b-jets.

	Run 2A	***Run 2B***
$\boldsymbol{P(n_b \geq 1)}$	68%	80%
$\boldsymbol{P(n_b \geq 2)}$	21%	35%

One can see from the table that an essential improvement in the selection of events with b-tagged jets can be achieved with the Run 2B tracker as compared to the existing tracker. Taking into account the lower mis-tagging rate obtained in the Run 2B geometry, one can conclude that the signal-to-background ratio in all analyses involving b-jets will be significantly better in the next run.

Because of the slight degradation of the track reconstruction efficiency in jets with increasing luminosity, the b-tagging efficiency per jet ($\varepsilon_{b)}$ deteriorates from 69% without pileup to 66% with an additional six minimum bias events. This leads to the slightly decreased values $P(n_b \geq 1)$=76% and $P(n_b \geq 2)$=33%. Mis-tagging rates were not seen to increase significantly at higher luminosity.

9.8 Conclusions

The Run 2B silicon detector demonstrates good physics performance in a realistic simulation that includes detailed physics and detector response modeling and full pattern recognition. The physics performance studies prove that the proposed silicon design meets the requirements of the physics program of DØ Run 2B.

The choice of small-degree stereo detectors leads to a significant decrease in ghost tracks and a consequent improvement in pattern recognition. The additional layer 5 at radius R=16 cm helps to improve p_T resolution for non-central tracks. The new layer 0 at a small radius results in a factor of 1.5 improvement in impact parameter resolution. As a consequence the single b-tagging efficiency per jet improves by 19% compared to that obtained with Run 2A; and the percentage of events with two b-tagged jets will be 14% higher than in Run 2A at a fixed mis-tagging rate.

Predictions made for discovery limits of the Higgs boson in Run 2B were based on the assumption that DØ would have the same performance as in Run 2A. The proposed silicon detector is shown to deliver even better performance for high-p_T processes.

[1] "MCFast Documentation Version v5_1", P. Avery *et al*, http://www-pat.fnal.gov/mcfast.html.

[2] http://www-d0.fnal.gov/newd0/d0atwork/computing/MonteCarlo/simulation/d0sim.html.

[3] J. Ellison and A. Heinson, "Effects of Radiation Damage on the DØ Silicon Tracker", DØ note 2679, July, 1995.

[4] A. Khanov, R. Demina "Histogramming Track Finding Algorithm Performance Study", DØ Note 3845.

[5] R. Field, "The Underlying Event in Hard Scattering Processes'', http://fnth31.fnal.gov/runiimc.

[6] A. Khanov, R. Demina "Histogramming Track Finder: The impact parameter b-tagging performance", DØ Note 3855.

CHAPTER 10 - BUDGET

The scope and timescale for building the DØ Run 2B silicon detector will require a tremendous amount of effort from the members of the collaboration as well as the engineers and technicians associated with them. The collaboration set up a Run 2B silicon study group in 2000 to start the specification and design stage for a new silicon tracker. Participation by many groups aided in forming a conceptual design and developing it to the point were we can now submit it as this TDR. During this time, a considerable effort has gone into simulations of the physics processes, thermal and mechanical studies, as well as electrical design studies. We have also benefited by analyzing the successes and failures in the Run 2A silicon detector design, the production of ladders, and their performance. The DØ Run 2B silicon group has also been aided by joint discussions with CDF. For instance, in the Fall of 2000, the readout chip was chosen to be the SVX4 chip so as to make a joint CDF-DØ chip. Joint discussions between the collaborations are formalized through a Silicon Run 2B Task Force which was setup by the Laboratory. We will continue to utilize this resource to help expedite the construction of our detector.

The Run 2B silicon detector project has been analyzed and put in a Work Breakdown Schedule (WBS). A cost estimate has been carried out based on this WBS structure. The Materials and Supplies (M&S) budget is summarized in Table 15. The total project cost is estimated to be slightly over $8M, with a contingency of about $3.4M. The readout system accounts for the largest fraction of the budget with $3.6M. This cost includes $0.5M for SVX4 chips, $0.7M for hybrids, $1.1M for cables, and $0.75M for various data acquisition cards. In addition $0.55M is budgeted for power supplies. There are three types of cables each accounting for about one-third of the cable cost: analog cables for layer 0, digital jumper cables which run from the hybrid to the junction card, and twisted pair cables which run from the junction card to the adapter card. The total silicon sensor budget is $2.2M. More than 2700 production sensors will be purchased as well as the necessary prototypes. The mechanical budget includes the costs for producing the layer 0 and 1 support structure at $0.4M, the layer 2-5 support infrastructure at $0.5M, and the beampipe for $0.225M.

WBS	**1.1**	**SILICON TRACKER**						
WBS	**ITEM**	**MATERIALS & SERVICES (M&S)**				**CONTINGENCY**		
1.1	**SILICON TRACKER**	**Unit**	**#**	**Unit Cost**	**M&S TOTAL**	**%**	**Cost**	**TOTAL Cost**
1.1.1	*Silicon Sensors*				2,244,400	31	703,320	2,947,720
1.1.2	*Readout System*				3,637,520	47	1,692,004	5,329,524
1.1.3	*Mechanical Design and Fabrication*				1,608,700	50	805,845	2,414,545
1.1.4	*Detector Assembly and Testing*				429,000	32	138,050	567,050
1.1.5	*Installation*				90,000	47	42,500	132,500
1.1.6	*Software*				51,000	22	11,400	62,400
1.1	**SILICON TRACKER**				**8,060,620**	**42**	**3,393,119**	**11,453,739**

Table 15 - M&S Cost Estimate

A successful proposal for an NSF Major Research Instrumentation grant was submitted in February of 2001 for this project. This grant will be managed by a consortium of 8 University groups: The University of Kansas (KU), Brown, California State University at Fresno (CSUF), Kansas State University (KSU), Michigan State University (MSU), State University of New York at Stony Brook (SUNY-SB), University of Illinois at Chicago (UIC), and University of Washington (UW). Foreign collaborators at CINVESTAV in Mexico and Moscow State University provided a substantial portion of the necessary matching funds. These groups, along with Fermilab, will form the core for the necessary manpower needed for the project. The Principal Investigator is Alice Bean (University of Kansas) who is also the Deputy Project Manager for the Run 2B silicon project. The grant provides for $1.68 million dollars from the NSF and almost $800K of matching money from the institutions involved to be funded over a three year period starting August 15, 2001. The funds from this grant will be managed under the Run 2B silicon project.

The timeline for completion of this project is very tight. In order to take advantage of the luminosity that the Tevatron will deliver, and be competitive with the LHC, we need to install the silicon detector into DØ in calendar year 2004. The group has proceeded to produce a resource loaded schedule in order to see how these deadlines can be met. To meet this schedule, silicon sensors will need to be ordered in late 2001 and delivered by mid-2003. Prototyping for all components needs to be completed by summer of 2002. The SVX4 chip development schedule calls for final delivery of chips in mid 2002 with prototype chips available by the end of 2001. These prototype chips will allow testing procedures to be finalized and hybrid design and prototyping to proceed. Module assembly and construction will start in the fall of 2002 to be in full swing during 2003.

CHAPTER 11 - SUMMARY

A design effort within DØ has been proceeding for the past two years to provide a new silicon detector capable of exploiting the physics potential available with the Tevatron Run 2B. The design studies for this new silicon detector were carried out within a set of boundary conditions set by the Laboratory. Even though these are significant, the new detector presented in this document is designed to have better performance than the Run 2A detector. The proposed silicon detector has a 6 layer geometry arranged in a barrel design. The detector will be built in two independent half-modules split at z=0. The six layers, numbered 0 through 5, are divided in two radial groups. There are a total of 2184 silicon sensors in this design, read-out with 888 hybrids containing 7440 SVX4 chips. For comparison, the Run 2A silicon detector has 793K readout channels while the Run 2B one will have 952K readout channels. The Run 2B silicon detector is designed to allow for faster construction due to fewer and simpler parts than the Run 2A device. With the new detector we will have better stand-alone silicon tracking. We have optimized our design to the extent possible to obtain a detector that is superior to the Run 2A detector and that will allow us to be well placed for the possibility of discovering new physics.

The physics performance studies prove that the proposed detector design meets the requirements of the physics program of DØ Run 2B. The choice of small-degree stereo detectors leads to a significant decrease in ghost tracks and thus improved pattern recognition. Layer 5 at a radius of 16 cm helps to improve the p_T resolution for non-central tracks. The new layer 0 at small radius results in a factor of 1.5 improvement in impact parameter resolution. As a consequence, the single b-tagging efficiency per jet improves by 19% compared to that obtained with Run 2A; and the percentage of events with two b-tagged jets at fixed mistag rate will be 14% higher than in Run 2A. Predictions made for discovery limits of the Higgs boson in Run 2B were based on the assumption that DØ would have the same performance as in Run 2A. The proposed detector is shown to deliver even better performance for high-p_T processes.

APPENDIX A - RUN 2B PROJECT MANAGEMENT

Most of the structure of the project management for Run 2B has been put in position during the past few months, with personnel assignments for the uppermost tier having been in place since June of this year. The current organization chart is shown in Figure 100. Jonathan Kotcher from Brookhaven National Laboratory is the Project Manager, with his selection having been approved by the Fermilab Directorate. Richard Partridge from Brown University is the Deputy Project Manager, with a term of one year. He will assist in all aspects of project development and management, with a special emphasis on guiding and overseeing the physics studies and simulations as the designs reach fruition. Much of the focus of the Run 2B upgrade is related to electronics and triggering elements. Marvin Johnson of Fermilab has agreed to serve as the Technical Coordinator, bringing an important set of skills and experience to many of the sub-projects we are pursuing. Bill Freeman of Fermilab will oversee the Run 2B Project Office, through which all upgrade schedule and cost development, accounting, and tracking will be managed.

The silicon sub-project organization is well established. Marcel Demarteau from Fermilab has agreed to serve as Silicon Sub-Project Manager, and has served in this capacity since June, 2001. Alice Bean from the University of Kansas is the Deputy Silicon Sub-Project Manager, and will serve for a term of one year. This latter assignment was made in early July. Further sub-divisions of the silicon sub-project, with their personnel assignments (where known), are shown in Figure 100. These sub-headings consist of mechanical; sensors; electronics; assembly/production; quality assurance, testing, and burn-in; simulation; and radiation monitoring. The few outstanding assignments will be made as preparations for detector fabrication become more intensive. The silicon management structure was developed over the summer, and the sub-project is maturing into an efficient, well-coordinated effort.

The remaining portions of the project at WBS level 2 are divided into the three trigger levels – Levels 1, 2 and 3 – the online system, and installation and infrastructure. Each of these subsystem managers, including the silicon sub-project managers, reports directly to the project management. All personnel assignments have been made at this level of the project, with the exception of that overseeing installation (this is commented on below). Hal Evans (Columbia University) and Darien Wood (Northeastern University) are managing the Level 1 trigger sub-projects. The Level 2 trigger is being managed by Robert Hirosky (University of Virginia) and Jim Linnemann (Michigan State University). Gerald Blazey (Northern Illinois University) and Paul Padley (Rice University) oversee the Level 3 system, and Stu Fuess (Fermilab) and Paul Slattery (University of Rochester) the upgrades to the online system. This mix of personnel represents a sought after balance between adopting new, fresh approaches on the one hand, and maintaining the historical base and some measure of technical continuity on the other. Evans, Wood, Hirosky, and Padley, while new to their roles as DØ WBS Level 2 sub-project managers, have each made very significant contributions to the experiment in past years in leadership roles in the hardware, and in various aspects of the software and physics. Linnemann, Blazey, Fuess, and Slattery were sub-project managers at different levels in the previous upgrade; their participation is of particular utility in maintaining continuity in the sub-projects they are overseeing.

We note that most of the issues related to installation and infrastructure for this upgrade are associated on the mechanical side with the staging, insertion, and alignment of the silicon detector into the bore of the solenoid, and on the electrical side with a relatively minor but finite amount of new infrastructure that will be needed to accompany the upgraded trigger hardware. With Run 2 now scheduled to last six or more years, long-term maintenance has also become more of a concern. At the moment, these issues are being developed and overseen within the associated sub-projects. Should it be decided as the project becomes more clearly defined during the coming months that a separate WBS Level 2 sub-system is needed to address these problems more directly, we will make the appropriate manpower assignments to the installation and infrastructure sub-project. In anticipation of this possibility, we have begun discussions with the principals who might be asked to oversee this effort.

Management positions associated with the various sub-projects at WBS level 3 are as shown in the organization chart. While most of the assignments have been made, three under the Level 1 trigger heading remain to be filled. These include the Level 1 calorimeter trigger upgrade, the Fiber Tracker Trigger (SIFT) chip replacement for 132 nsec running, and a possible upgrade to the Level 1 tracking trigger to accommodate high luminosity data taking. We are following the recently submitted recommendations of the Run 2B Trigger Upgrade Task Force as we define and finalize these projects. Intial design work and, in the case of the SIFT replacement, an initial chip submission, are underway in all of these cases, as are discussions with potential contributing institutions (from both the United States and France) and possible sub-project managers. We direct the reader to the Trigger Conceptual Design Report for more details about the status of these and other WBS Level 3 trigger sub-projects.

An understanding of the role, charge, and scope of responsibility of each of the principals chosen to lead the various portions of the upgrade project has been reached between the relevant parties. More detailed descriptions of these and other roles will be contained in writing in the Project Execution Plan, which is being prepared for submission on November 15 to the Laboratory. We also note that the Run 2B upgrade described here includes Run 2A trigger sub-projects that have not yet been completed. The project management structure shown was created in order to help ensure coherent, centrally managed oversight of all projects required for the accumulation of 17 pb^{-1} or more during the whole of Run 2 – Run 2A + 2B. Successful completion of all of the sub-projects is essential for attaining our physics goals; we therefore believe it is essential to treat them all on an equal footing from the outset as the new project is defined. Further details on this issue can be found in the introduction to the Trigger Conceptual Design Report.

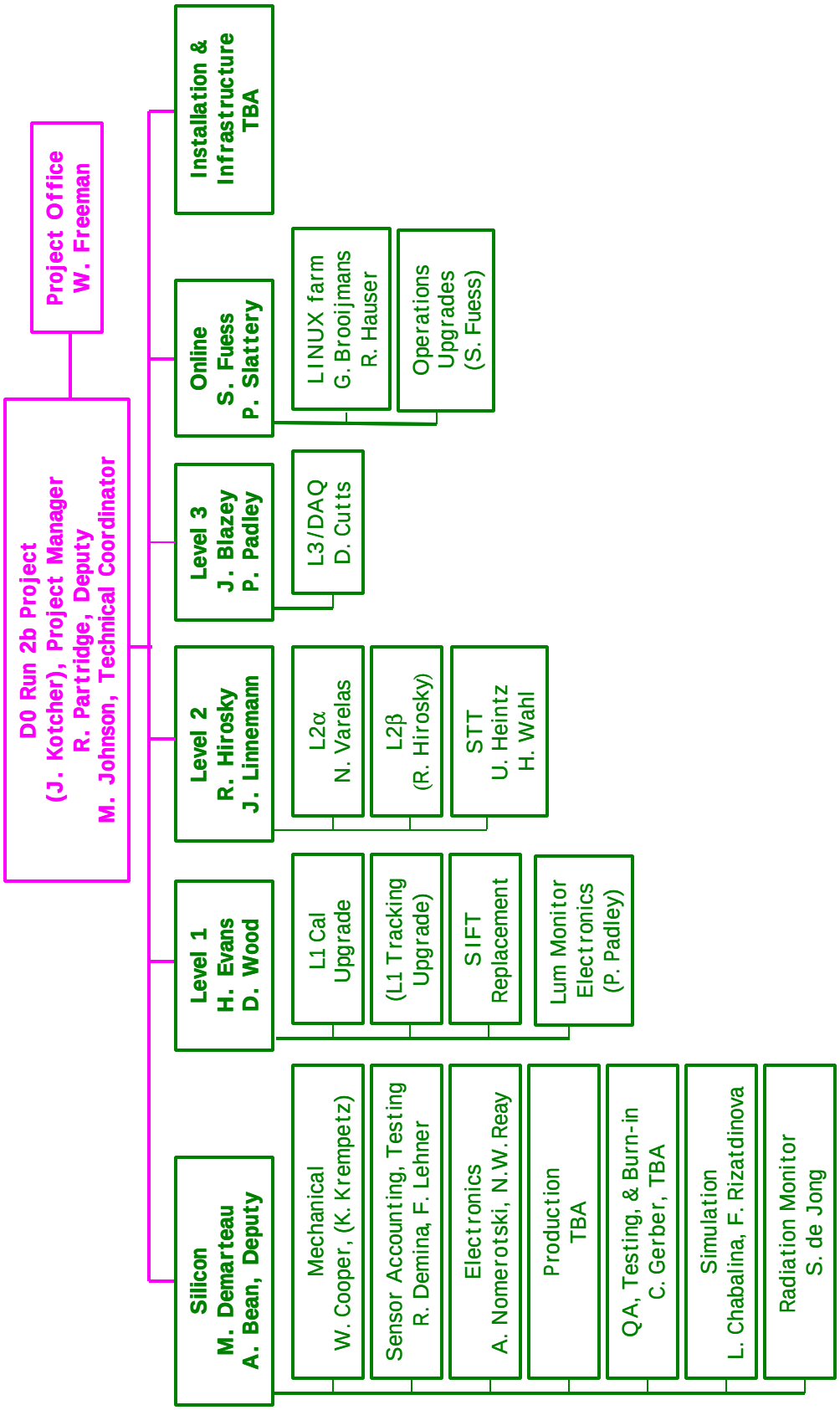


Figure 100- Run 2B Project Organization